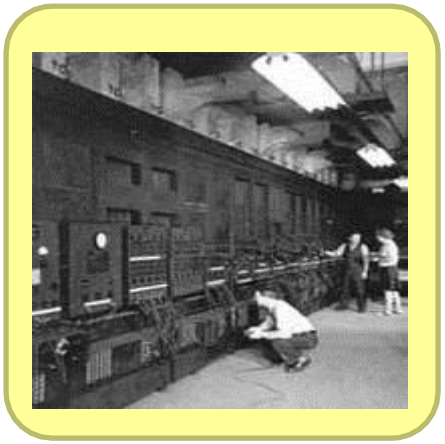
# Implementación de Sistemas Electrónicos

- Un poco de historia, evolución tecnológica
- Fabricación y diseño de C.I CMOS.
- Opciones de diseño
- Flujo de Diseño

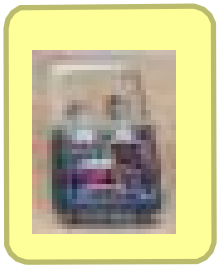
# Historia y evolución tecnológica

## 1946. ENIAC-Electronic Numerical Integrator And Computer.



The first electronic “ENIAC” computer

Vacuum lamp



First generation electronic modules

- 2,4 m x 0,9 m x 30 m  27 Toneladas
- 160KW
- 1.5 Mflops

# Historia y evolución tecnológica

1948. Primer transistor en los Bell Labs

# Historia y evolución tecnológica

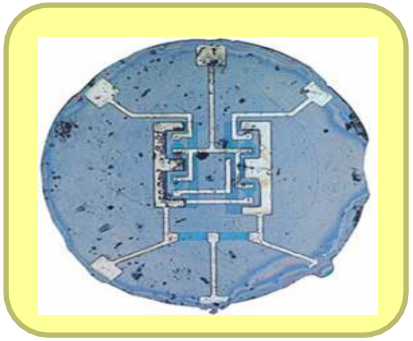
1954. Primer computador con transistores

Computador

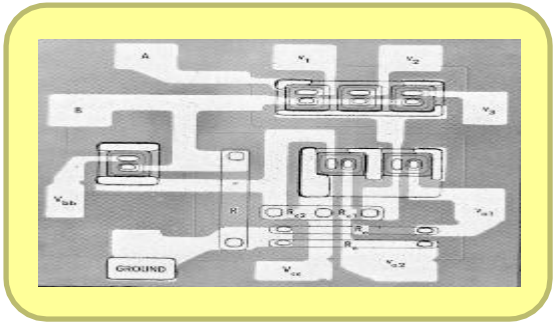
Transistores individuales BJT

# Historia y evolución tecnológica

## 1961. Primer circuito integrado



TI and Fairchild introduce the first logic ICs

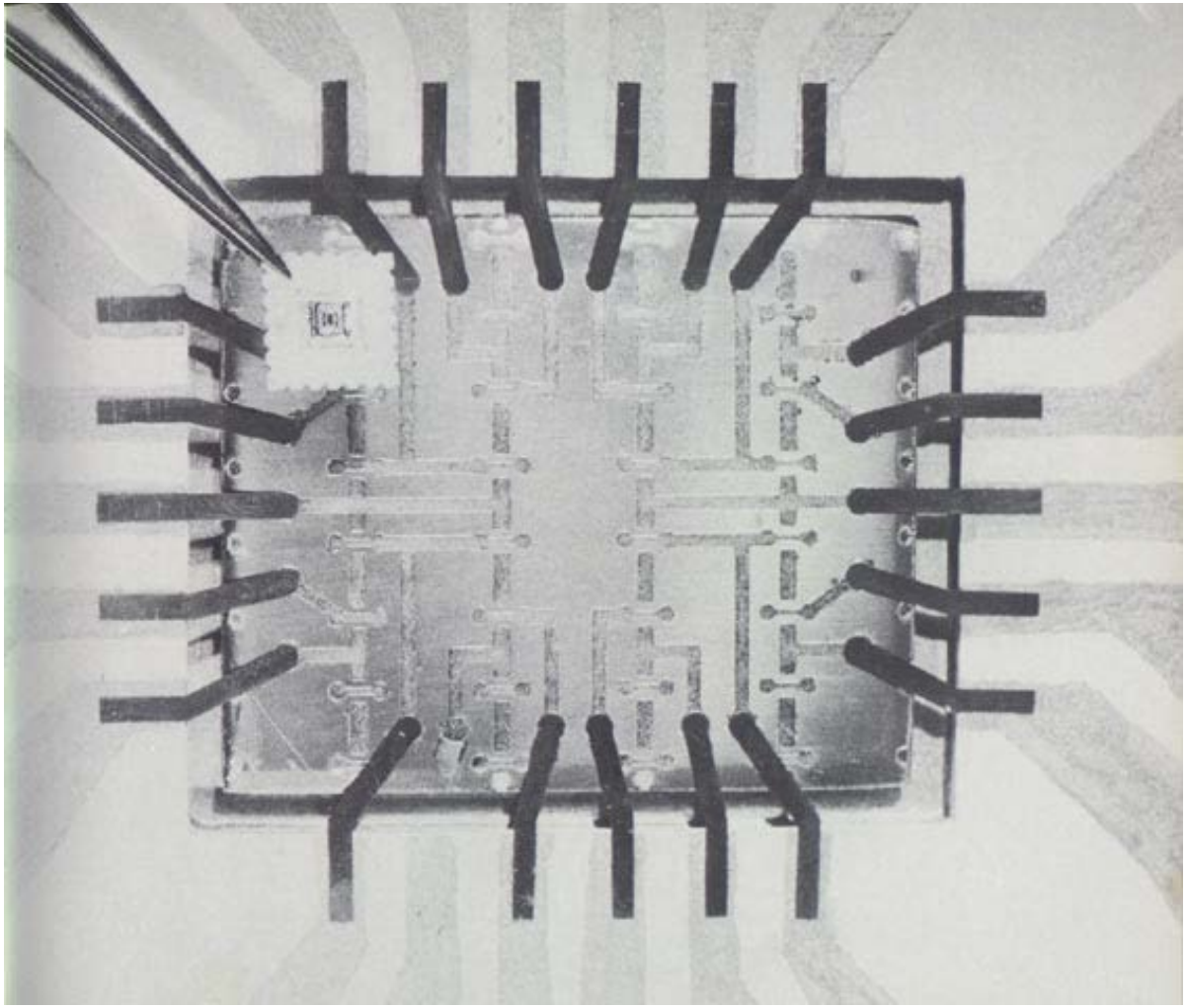



3-input Gate, which in 1966 was manufactured by Motorola

- Solo unos pocos transistores
- Muy muy caros $50

# Historia y evolución tecnológica

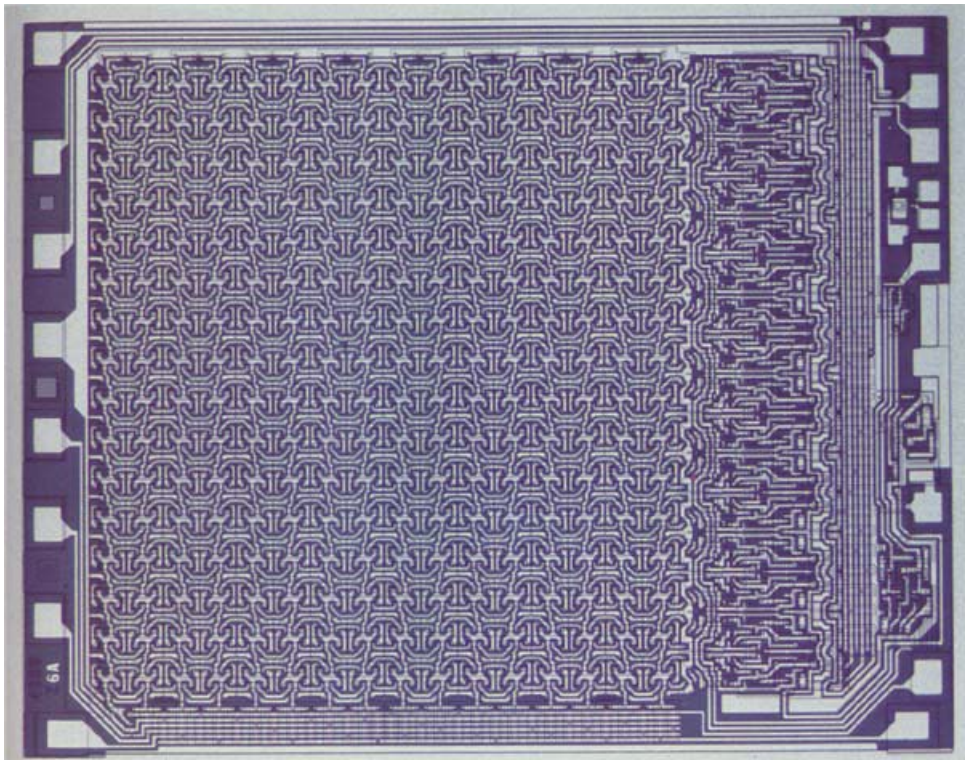
1962. Primer transistor MOS



# Historia y evolución tecnológica

1970 Primera 256-bit Static Random Access Memory (SRAM)

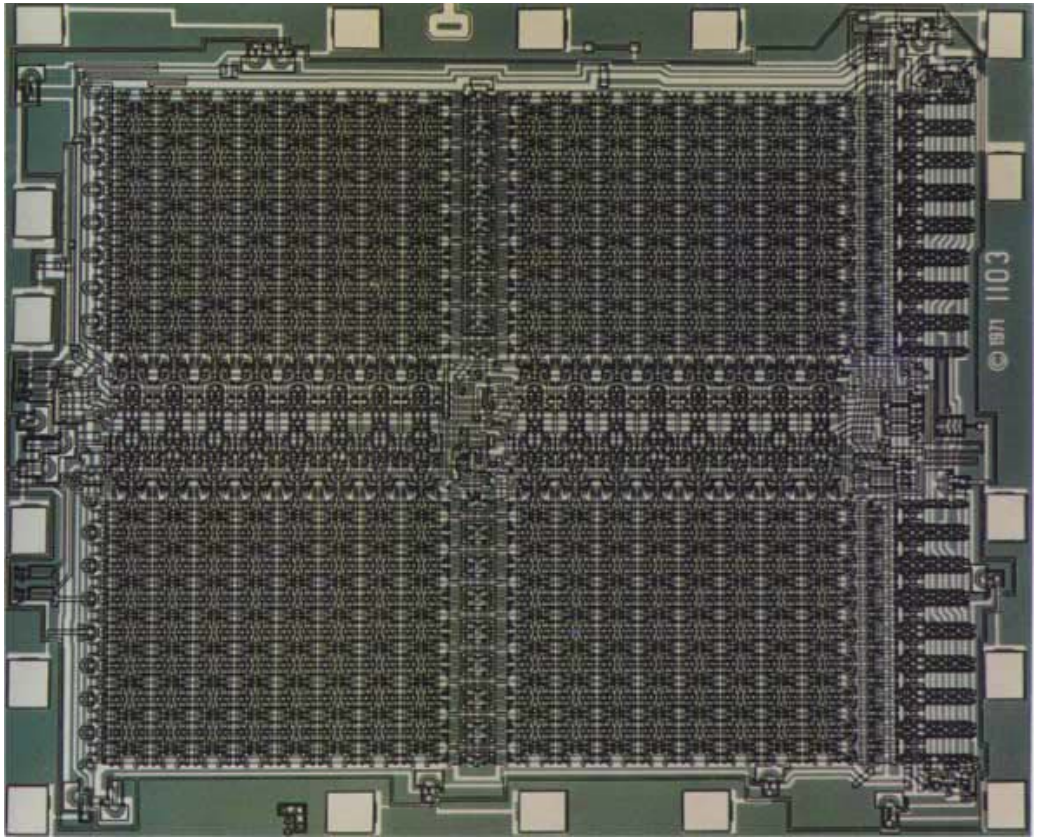
Fairchild 4100 256-bit SRAM



# Historia y evolución tecnológica

1970 1K-bit Dynamic RAM (DRAM)

Intel 1103 1K-bit DRAM

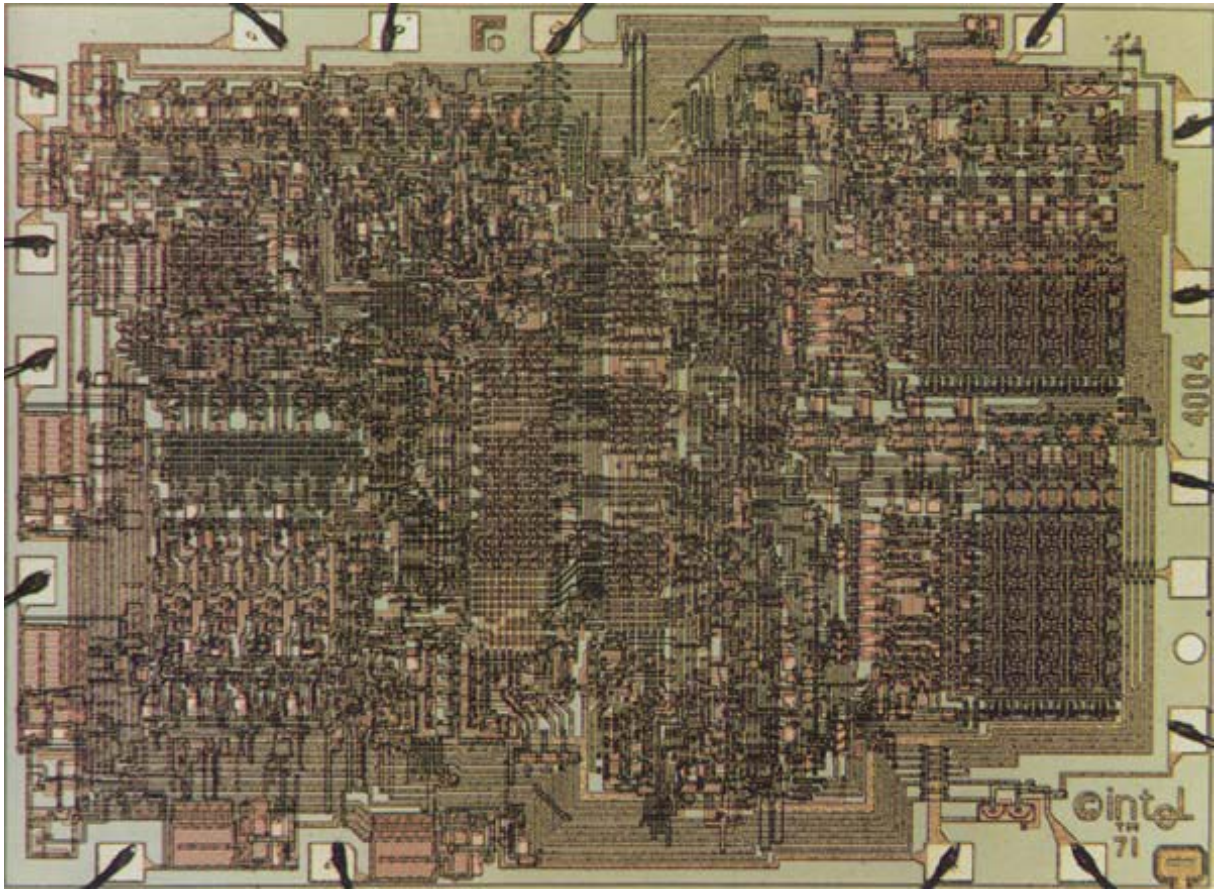


# Historia y evolución tecnológica

1971 Primer microprocesador

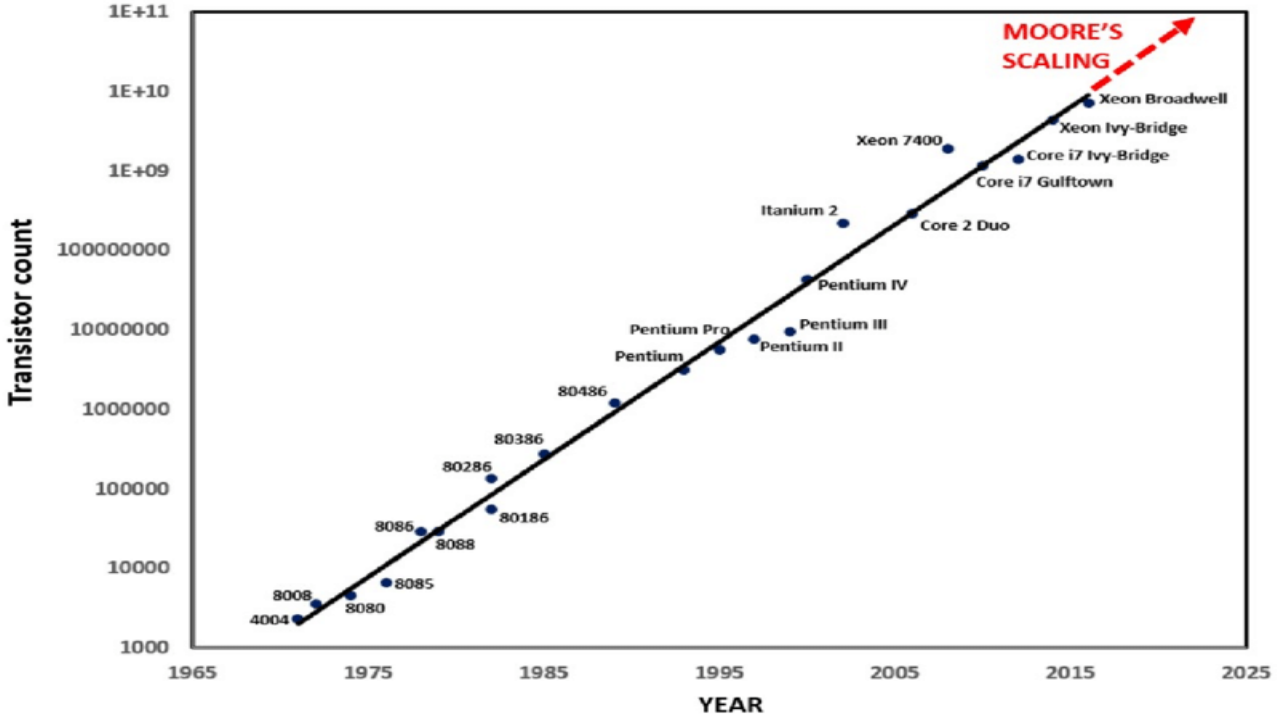
2300 transistores a 1 MHz

Intel 4004 Microprocessor



# Historia y evolución tecnológica

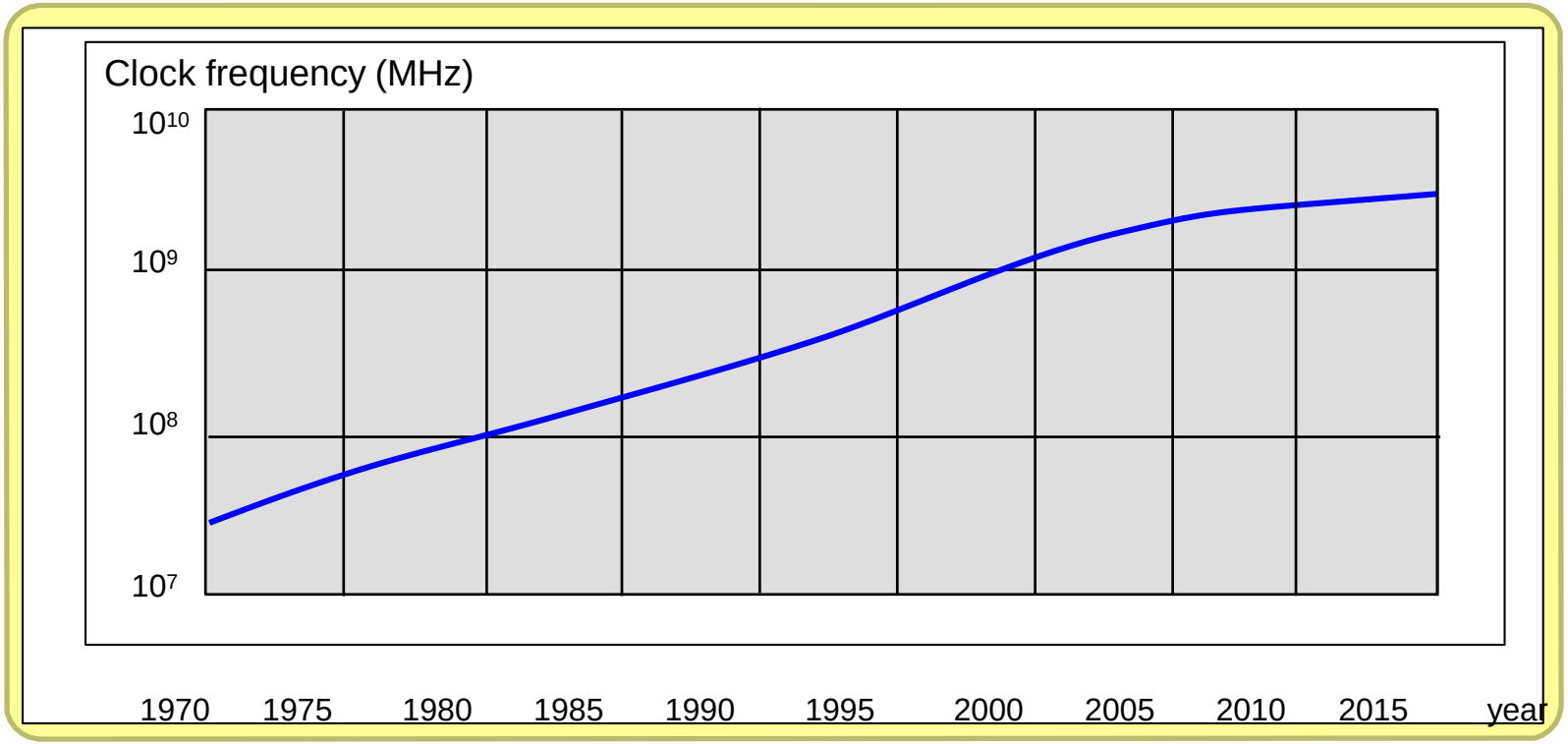
1975. Ley de Moore: La capacidad de integración se multiplica cada 18 meses




Los chips actuales ya tienen mas de 1000 millones de transistores

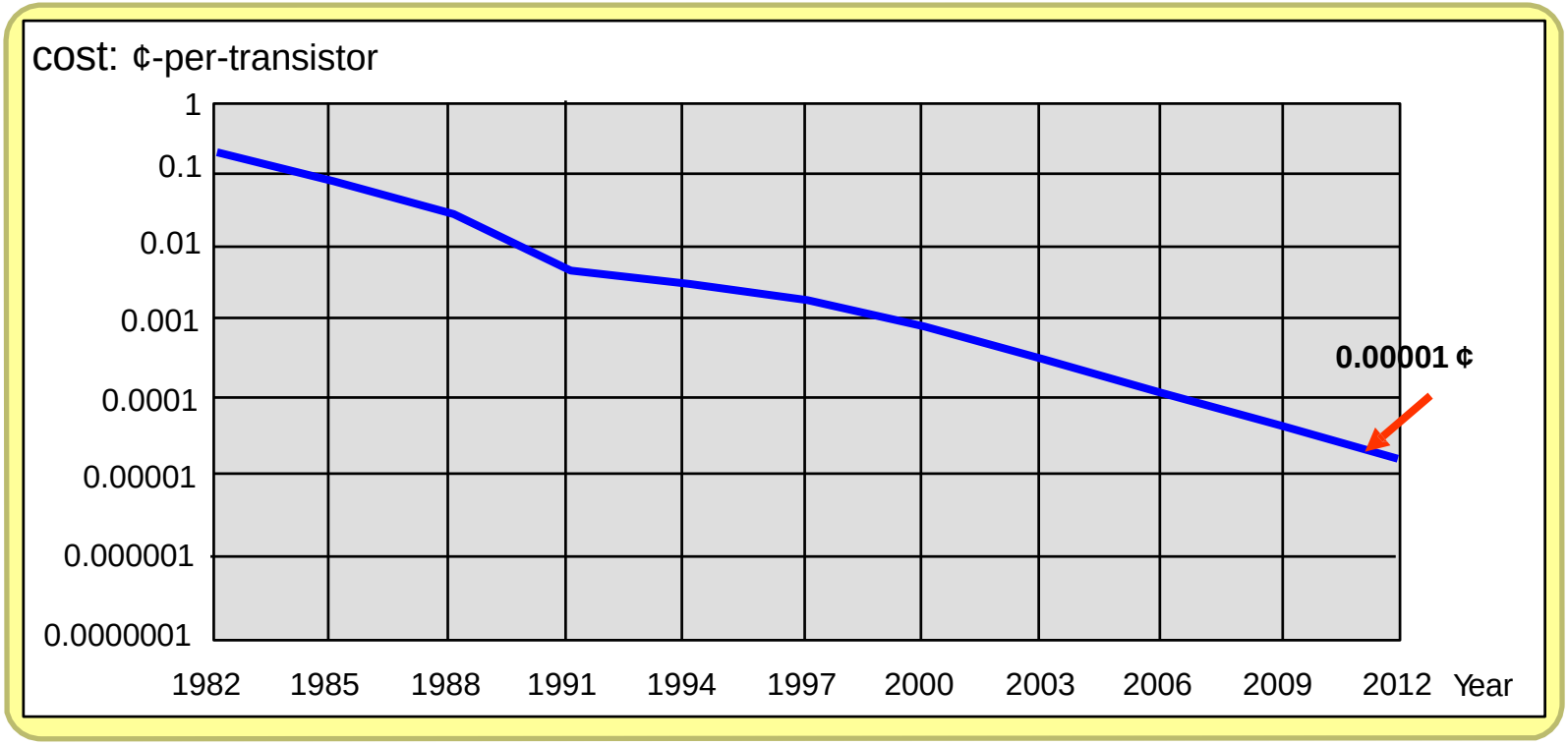
# Historia y evolución tecnológica

La frecuencia de reloj se multiplica por dos cada 2 años



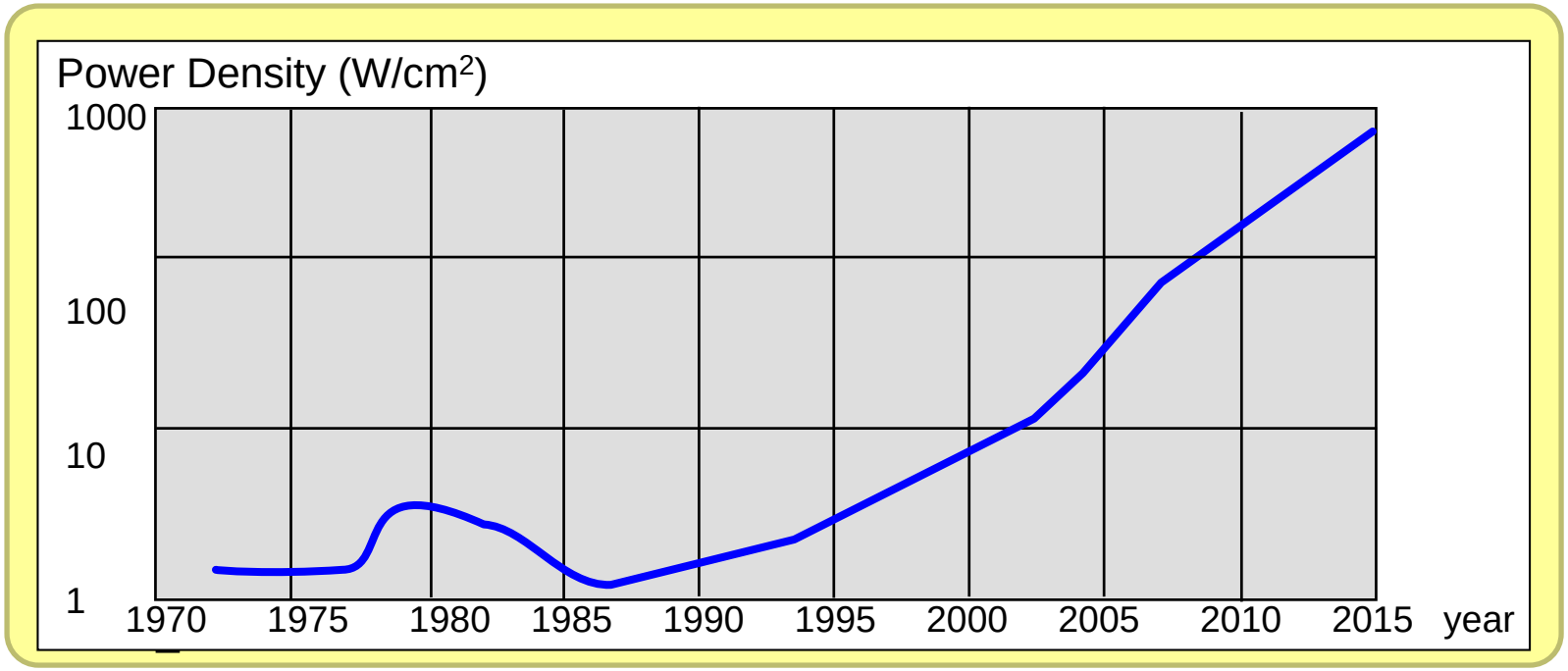
# Historia y evolución tecnológica

El coste de un transistor de divide por dos cada 1.5 años



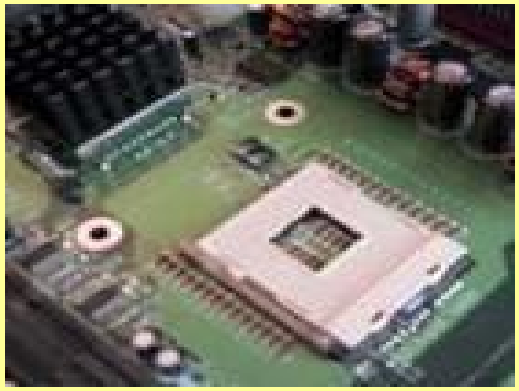
# Historia y evolución tecnológica

La densidad de potencia se multiplica por 2 cada año



# Historia y evolución tecnológica

**2000. Pentium IV**



- Technology: 180nm
- Contains 42 mln transistors
- 2 GHz operation

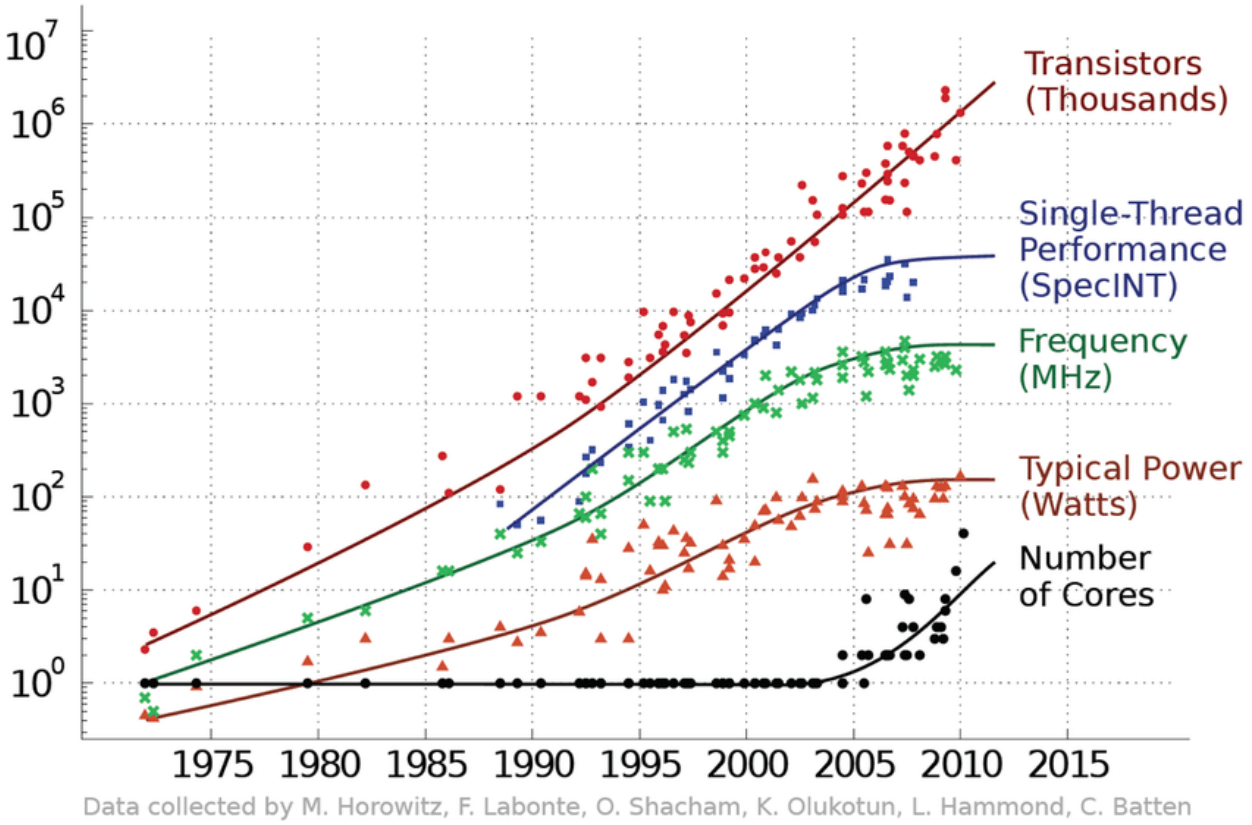
**2006. Core 2 Duo**


- Technology: 65nm
- Contains 291 mln transistors
- 2x3.2 GHz operation

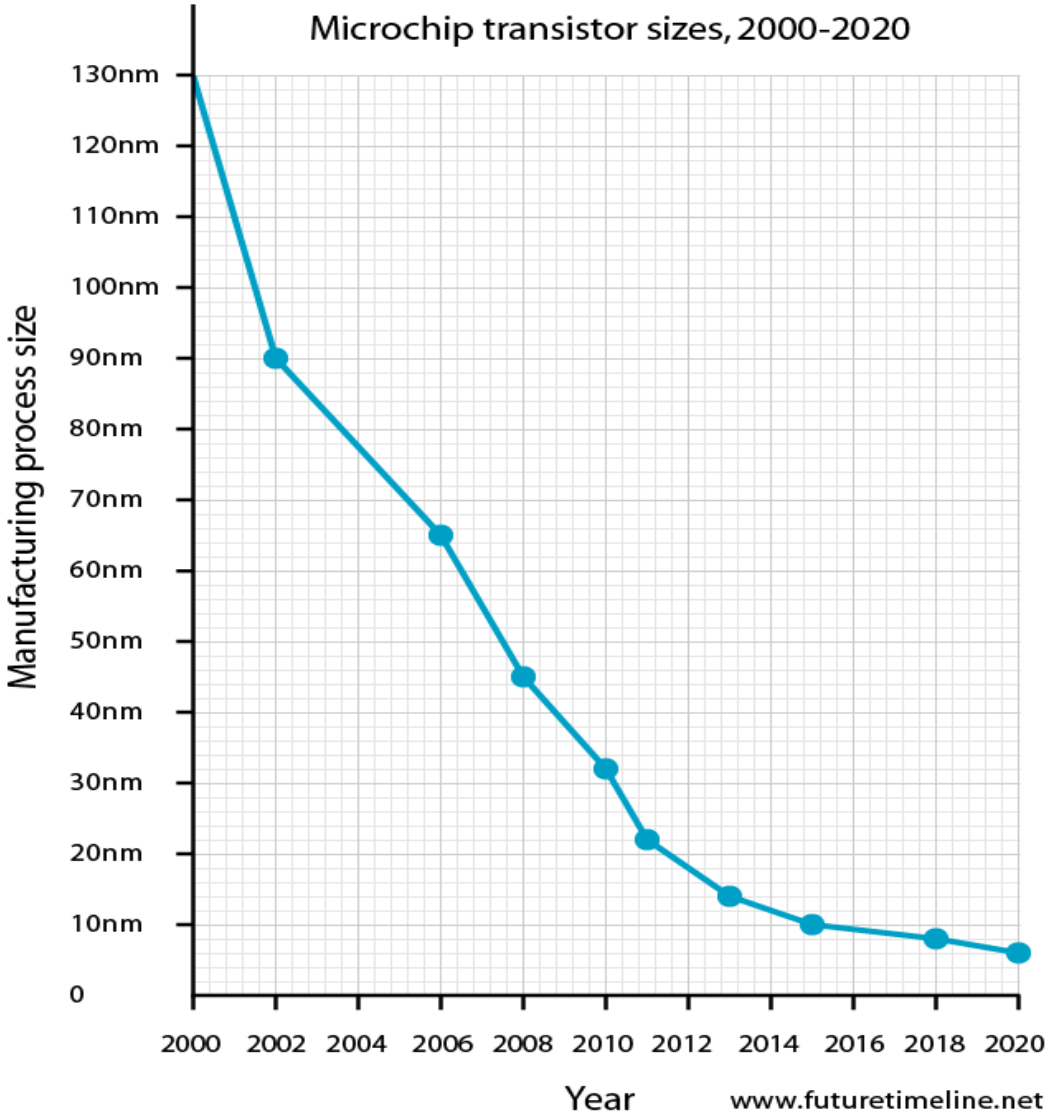
**2010. Xeon 7500**


- Technology: 45nm
- Contains 2.3 bln transistors
- 8x2.6 GHz operation

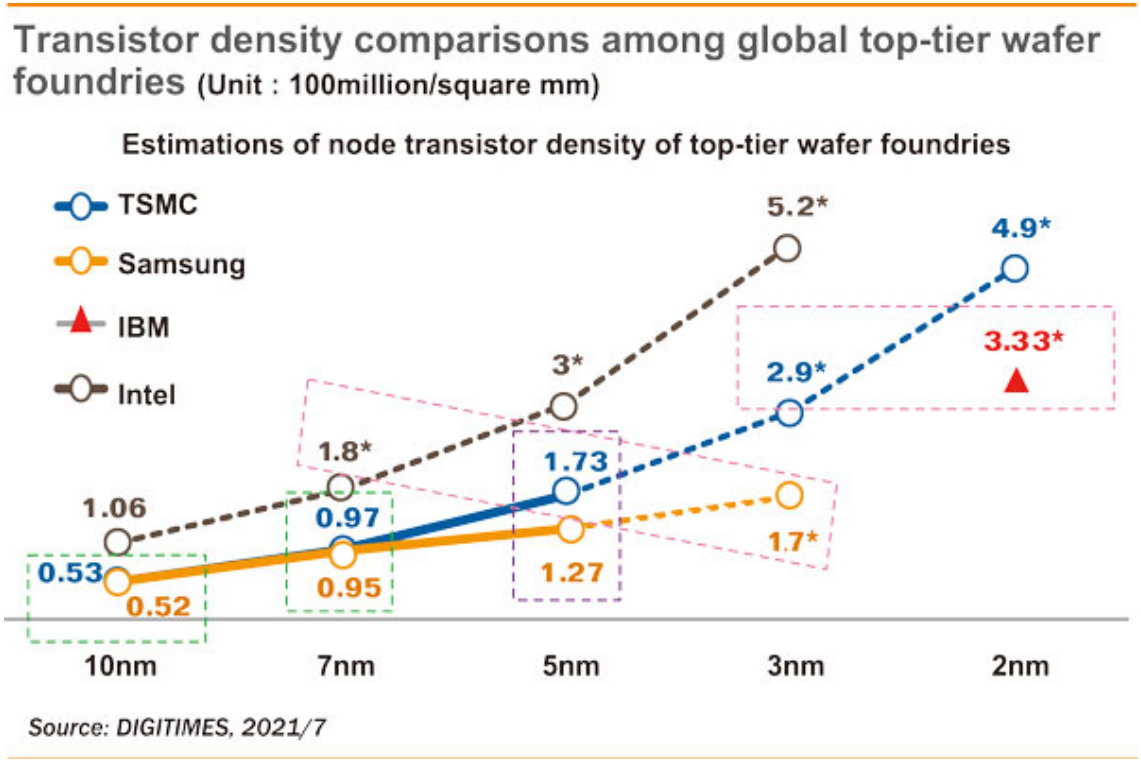
# Historia y evolución tecnológica



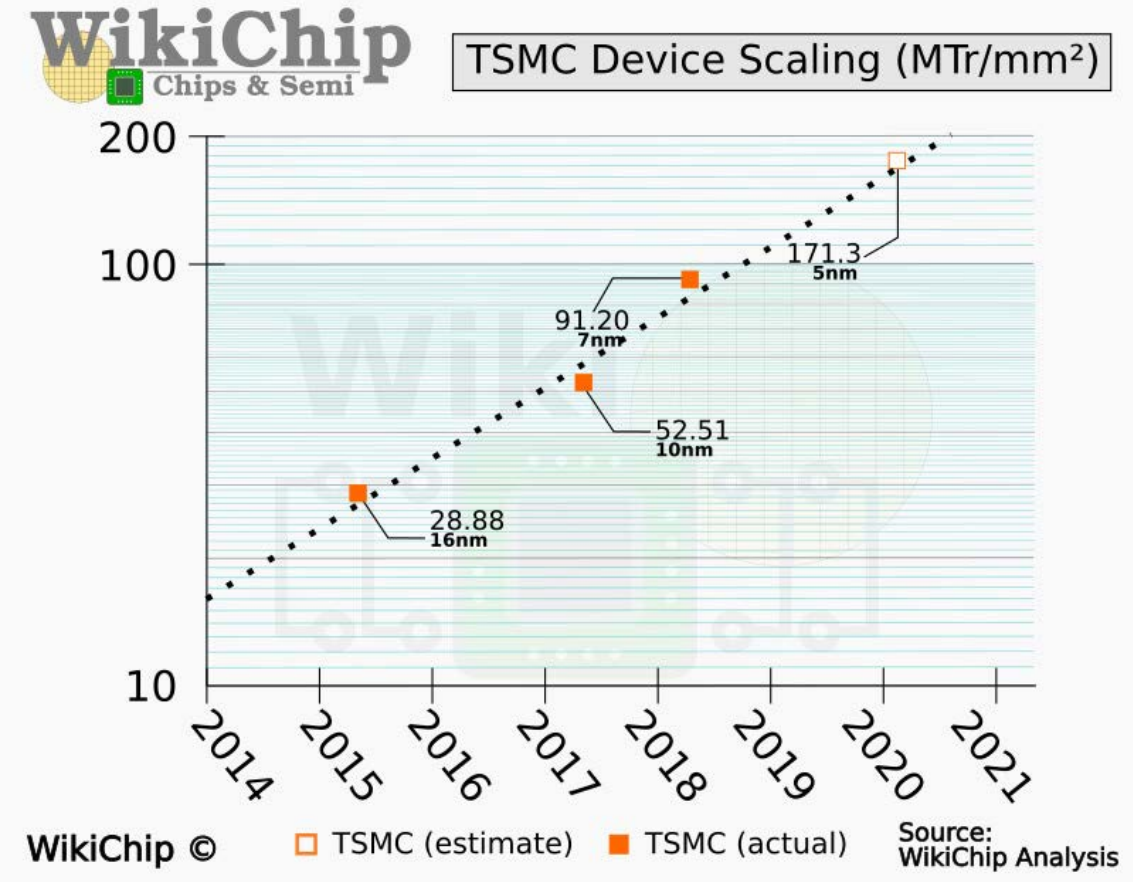
# Historia y evolución tecnológica



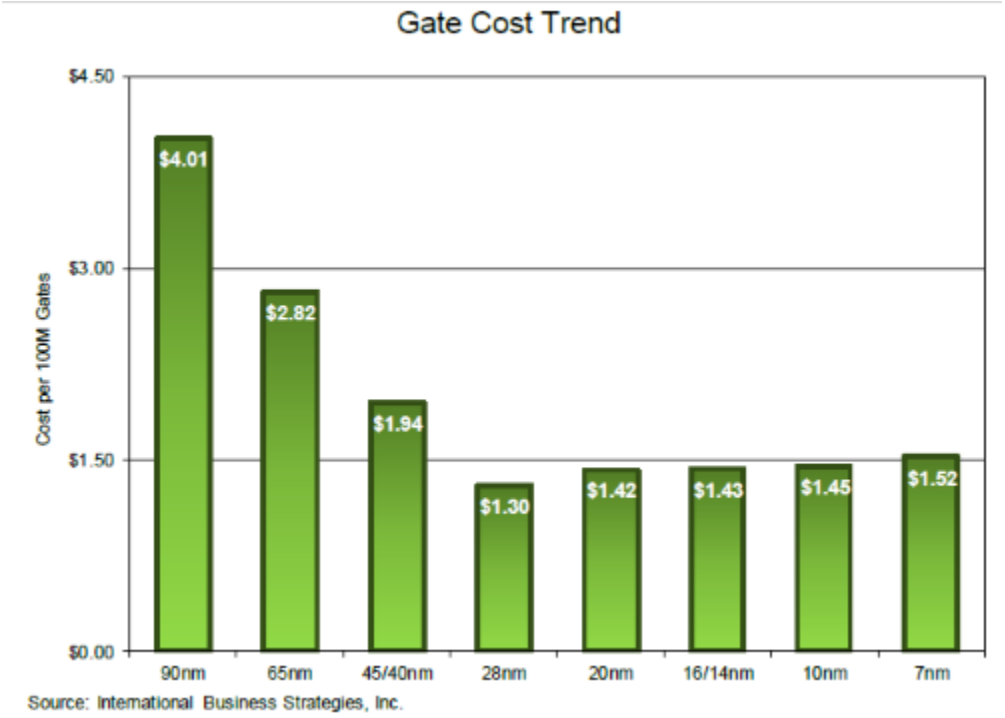
# Historia y evolución tecnológica



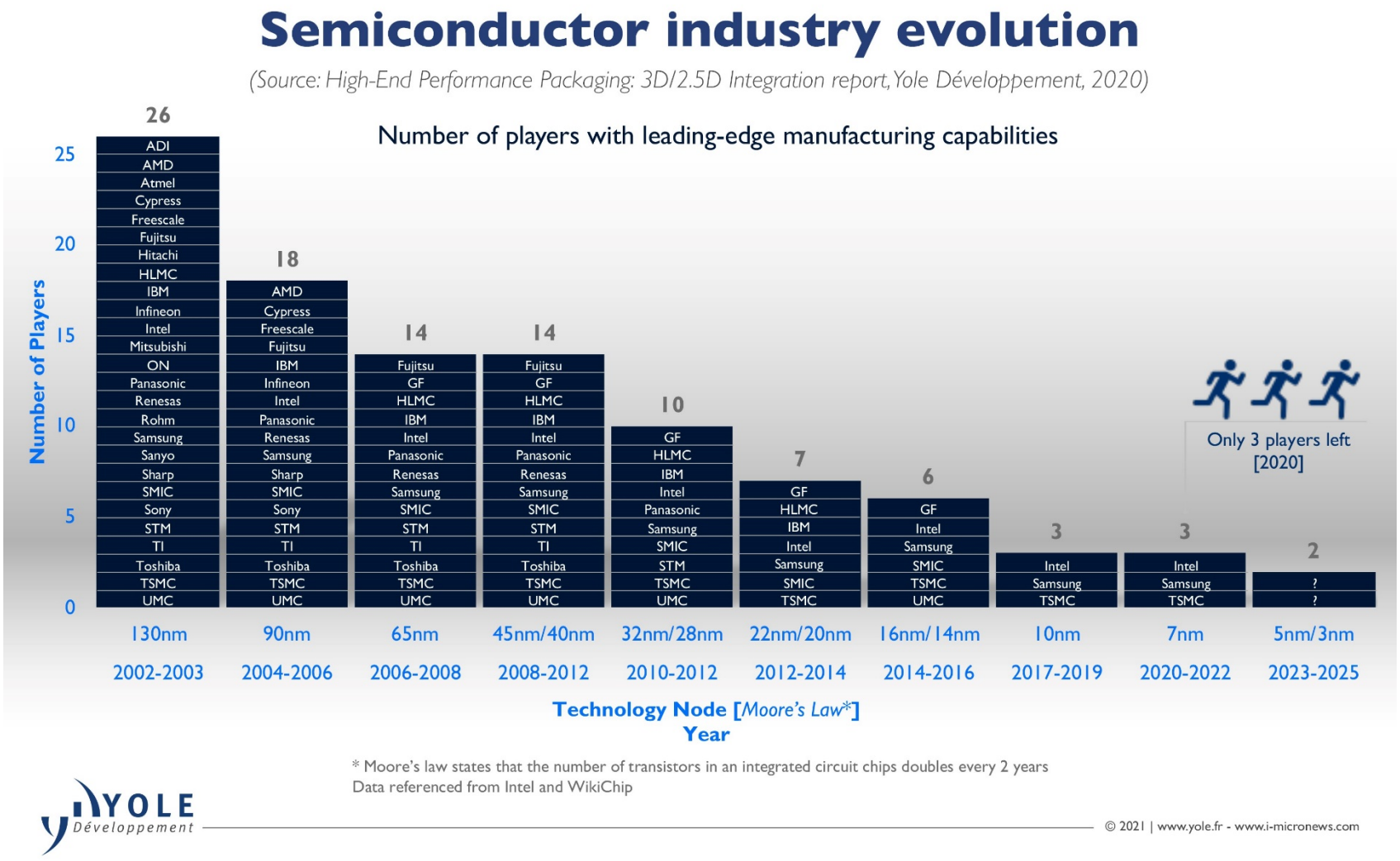
# Historia y evolución tecnológica



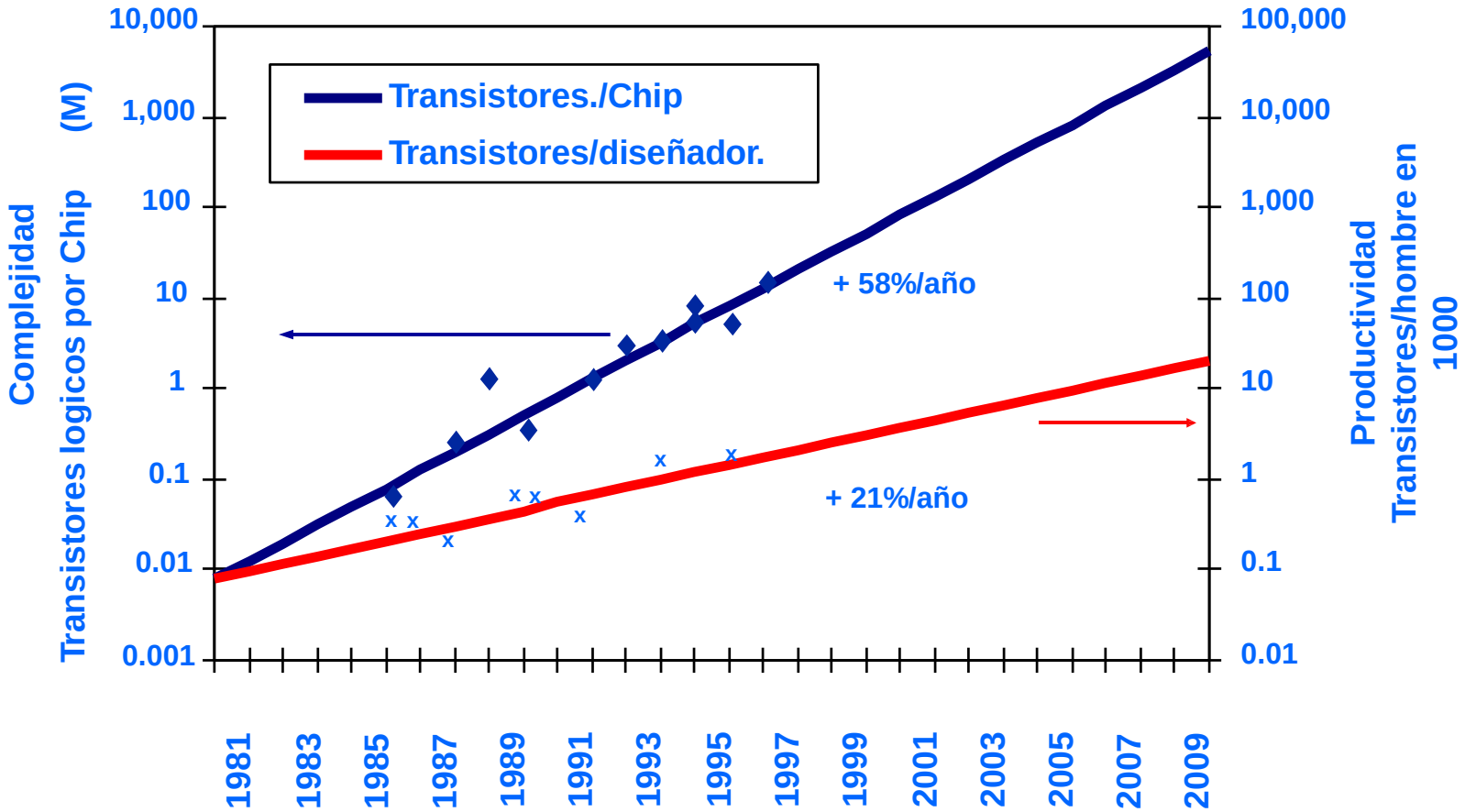
# Historia y evolución tecnológica



# Historia y evolución tecnológica



# Productividad




**Complejidad crece mas que la productividad**

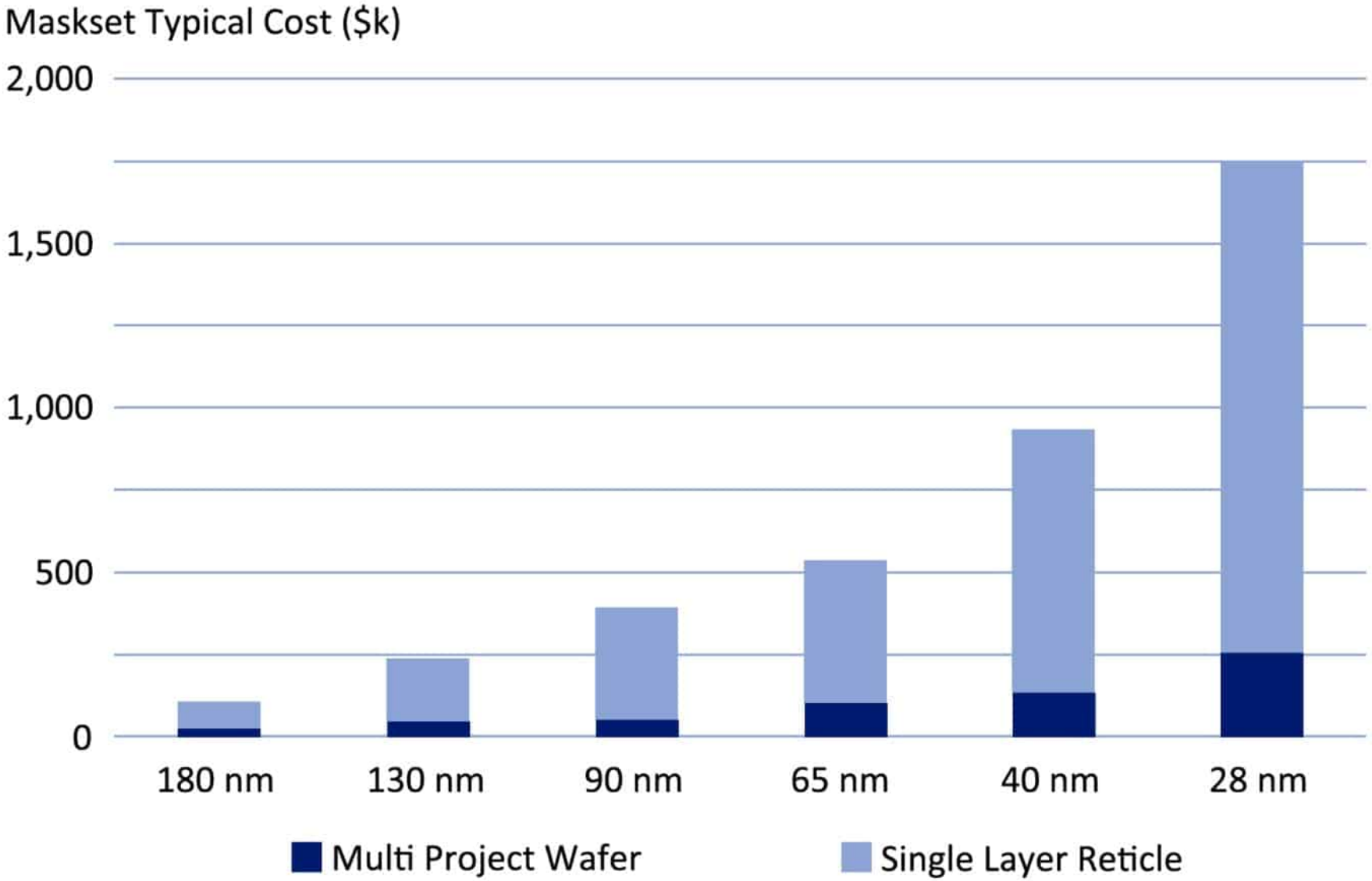


Courtesy, ITRS Roadmap

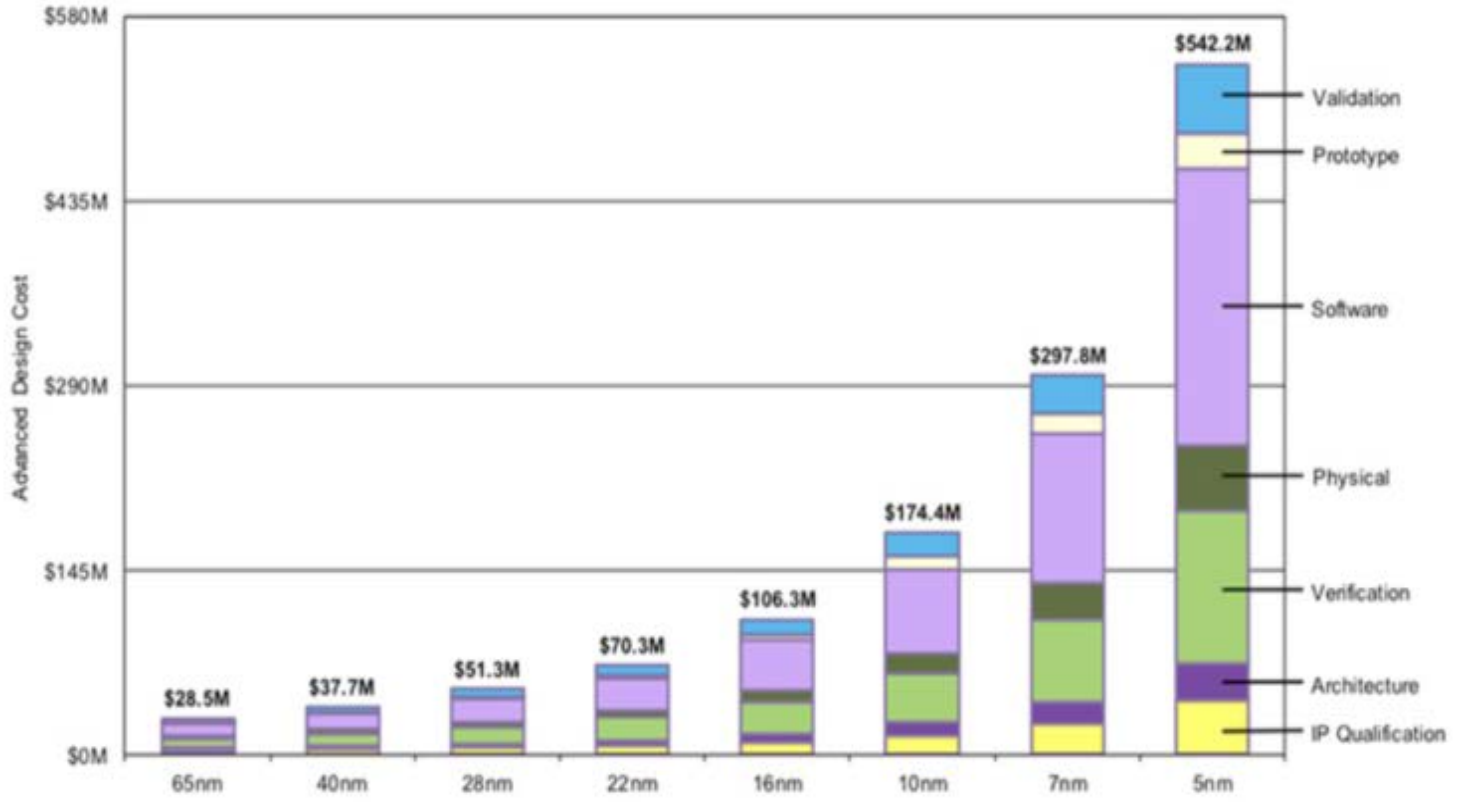
# Coste de un C.I.

- NRE (non-recurrent engineering) Prototipos
  - Diseño
  - Mascaras
- Produccion
  - Procesado del silicio, encapsulado, test
  - proporcional al volumen
  - proporcional al tamaño

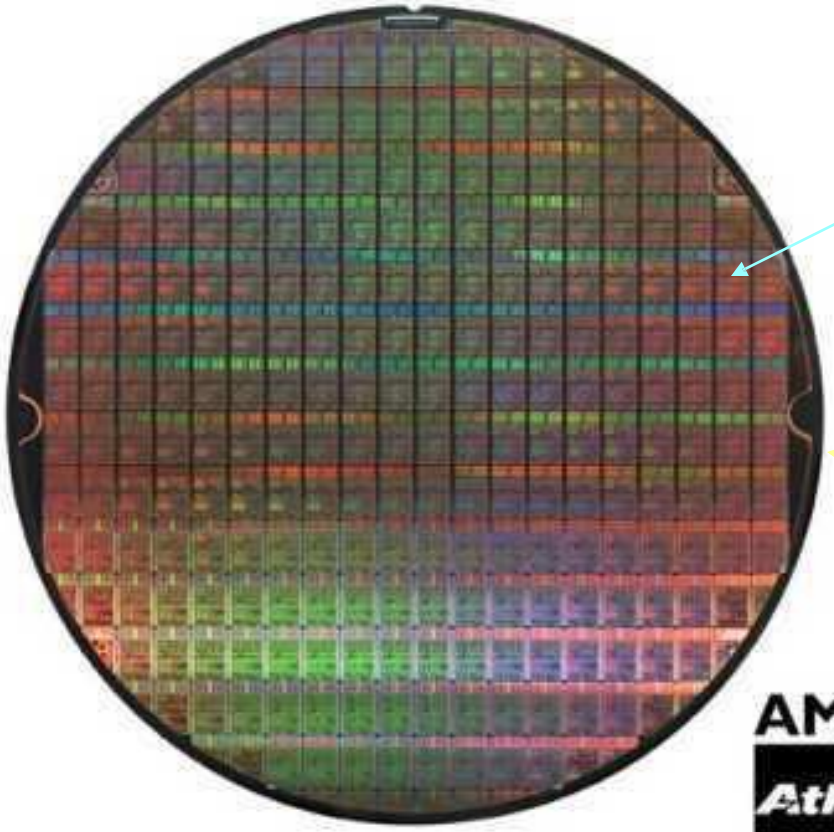
# Coste de los Prototipos



# Coste Total


$580M
$435M
$290M
$145M
$0M
Advanced Design Cost
$28.5M
$37.7M
$51.3M
$70.3M
$106.3M
$174.4M
$297.8M
$542.2M
65nm
40nm
28nm
22nm
16nm
10nm
7nm
5nm
Validation
Prototype
Software
Physical
Verification
Architecture
IP Qualification

# Coste de un chip



circuito

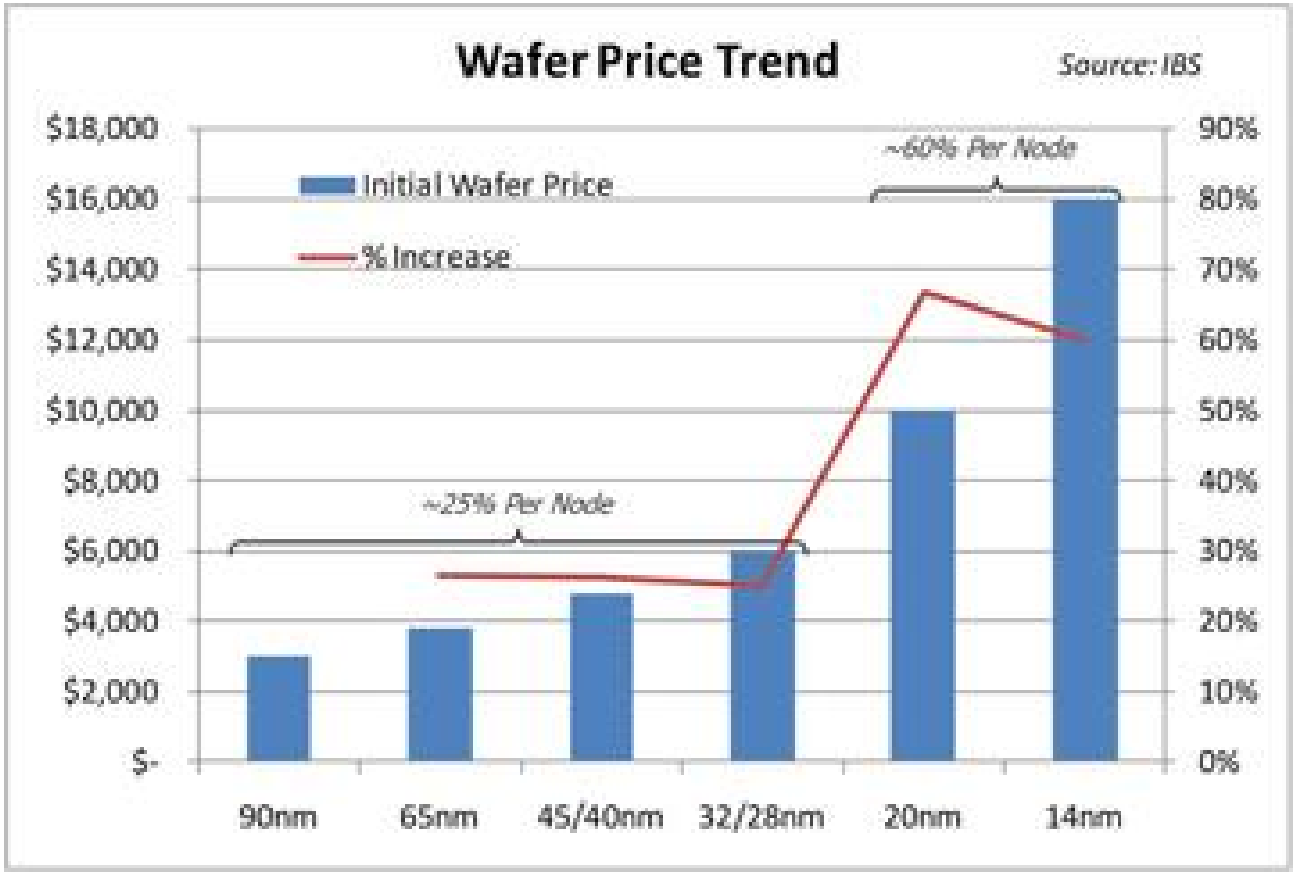
oblea

AMD Athlon

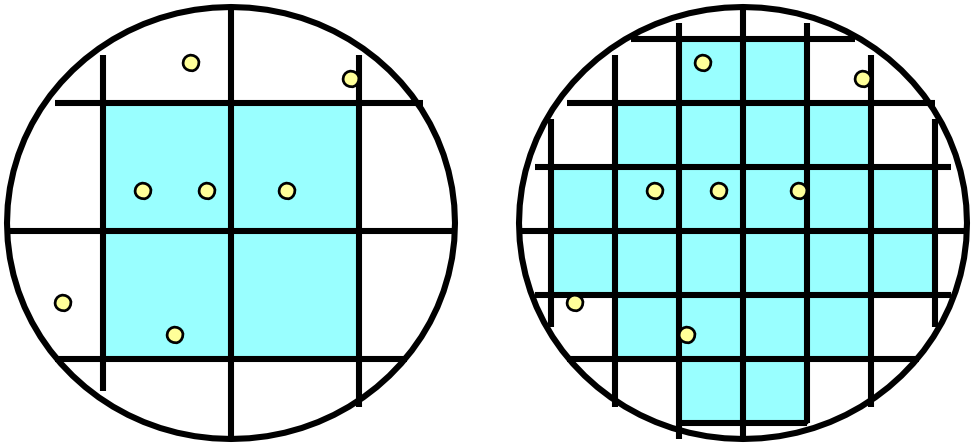
hasta 12” (30cm)

From http://www.amd.com

# Coste de una oblea



# Rendimiento



$$\text{coste chip} = f(\text{area chip})^4$$

# Coste por chip

| Chip | Metales | Anchura pistas | coste oblea | Def./ $cm^2$ | Area $mm^2$ | Piezas/ oblea | rendimiento | Coste/chip |
|---|---|---|---|---|---|---|---|---|
| 386DX | 2 | 0.90 | $900 | 1.0 | 43 | 360 | 71% | $4 |
| 486 DX2 | 3 | 0.80 | $1200 | 1.0 | 81 | 181 | 54% | $12 |
| Power PC 601 | 4 | 0.80 | $1700 | 1.3 | 121 | 115 | 28% | $53 |
| HP PA 7100 | 3 | 0.80 | $1300 | 1.0 | 196 | 66 | 27% | $73 |
| DEC Alpha | 3 | 0.70 | $1500 | 1.2 | 234 | 53 | 19% | $149 |
| Super Sparc | 3 | 0.70 | $1700 | 1.6 | 256 | 48 | 13% | $272 |
| Pentium | 3 | 0.80 | $1500 | 1.5 | 296 | 40 | 9% | $417 |

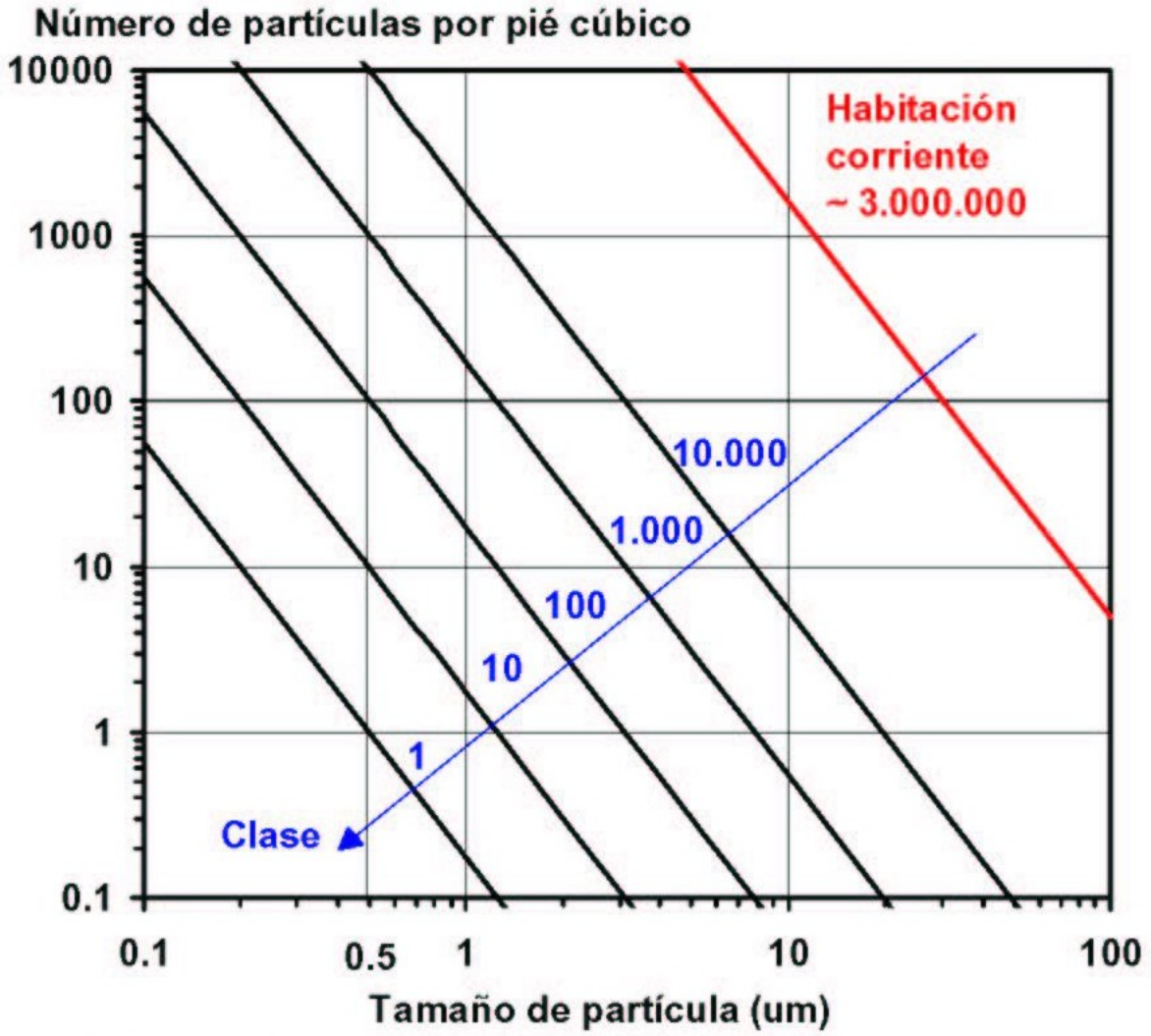
# Implementación de Sistemas Electrónicos

- Un poco de historia, evolución tecnológica
- Fabricación y diseño de C.I CMOS.
- Opciones de diseño
- Flujo de Diseño

# Foundry mediana

# Proceso de fabricación

# Salas blancas: clase (US std)




Clase:

1000 mediados 1970
100 mediados 1980
10 comienzos 1990
1 mediados 1990

# Salas blancas

- **Control**
  - + limpieza: partículas de polvo
  - + temperatura: 21 ± 1 ºC
  - + humedad: 40 ± 10 %
- **Vestuario especial**
- **Servicios**
  - + Aire acondicionado
  - + Aire comprimido
  - + Vacio
  - + Agua desionizada
  - + Gases ultrapuros
  - + Tratamiento de residuos

# Crecimiento de los lingotes de silicio

# Planarizacion:  Puliendo la oblea

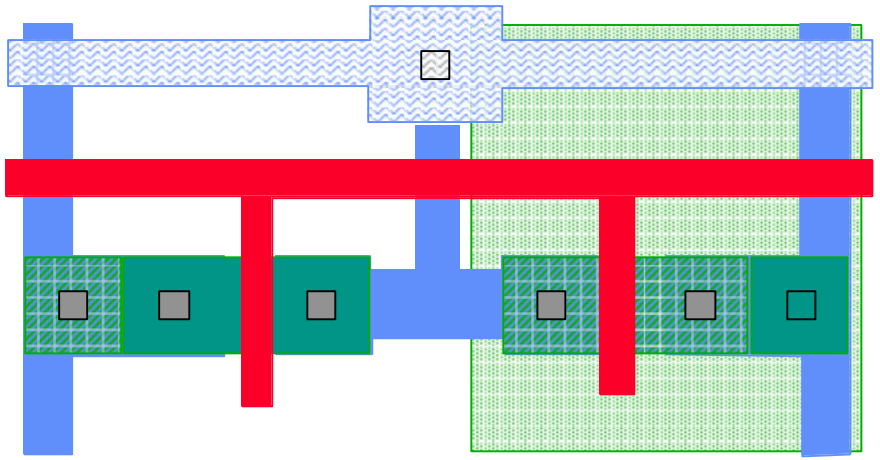
From *Smithsonian*, 2000

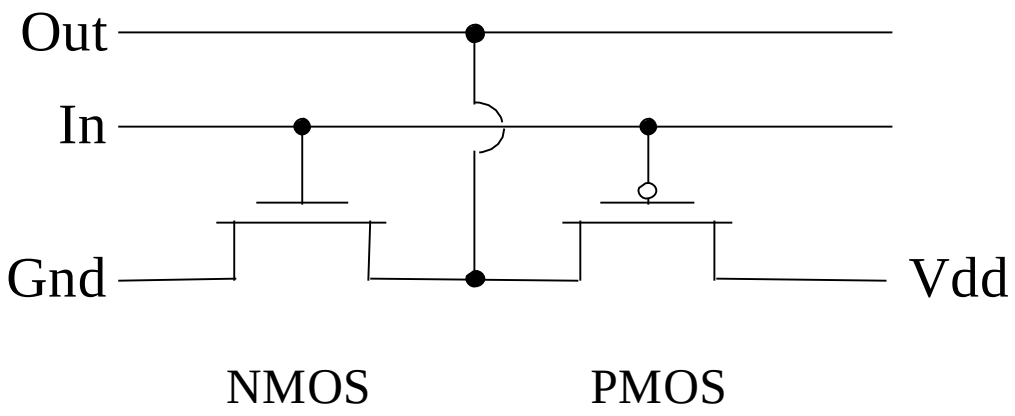
# Inversor CMOS

Layout:

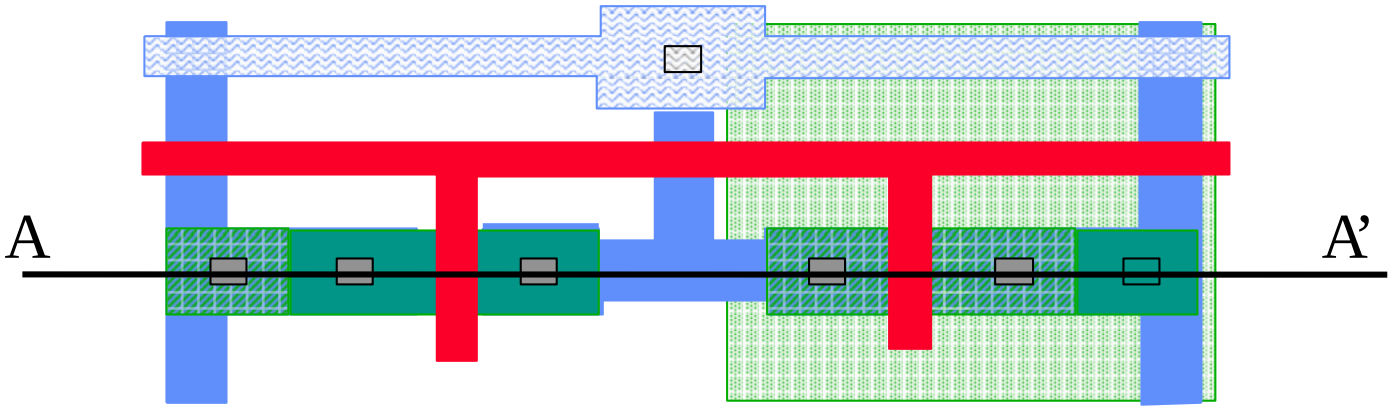
Leyenda:

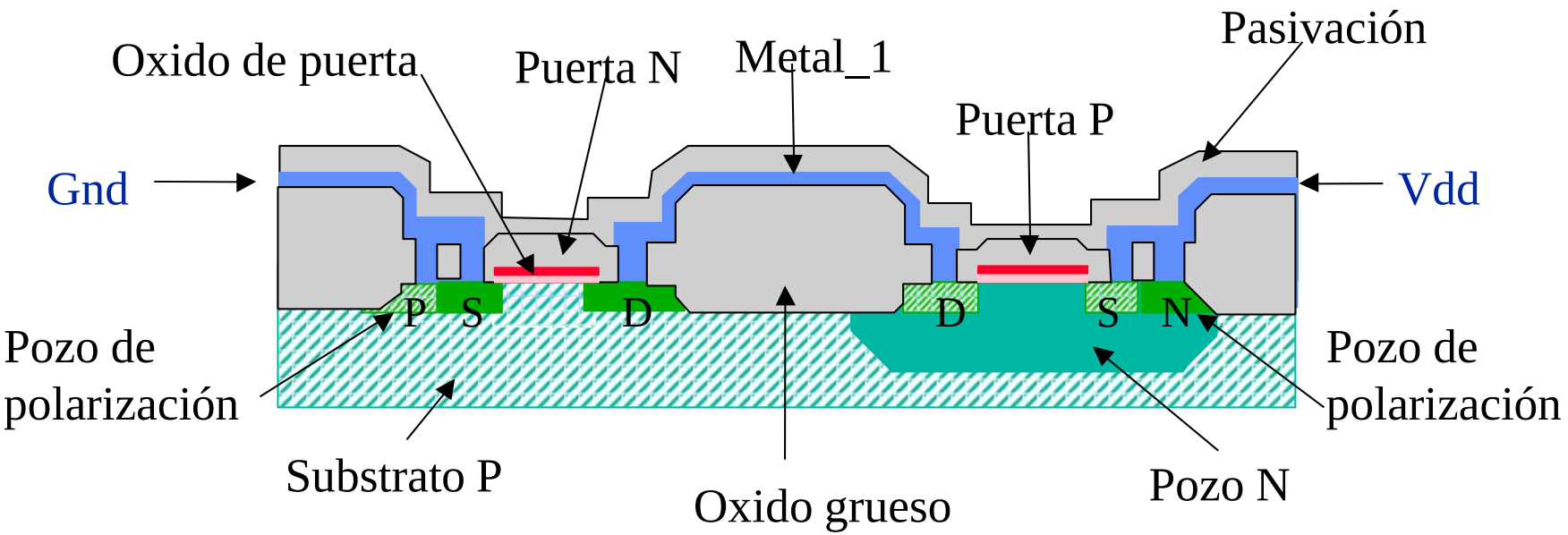
- Metal 2
- Via Metal
- 1
- Contacto
- Polisilicio
- Difusión N
- Difusión P
- Pozo N



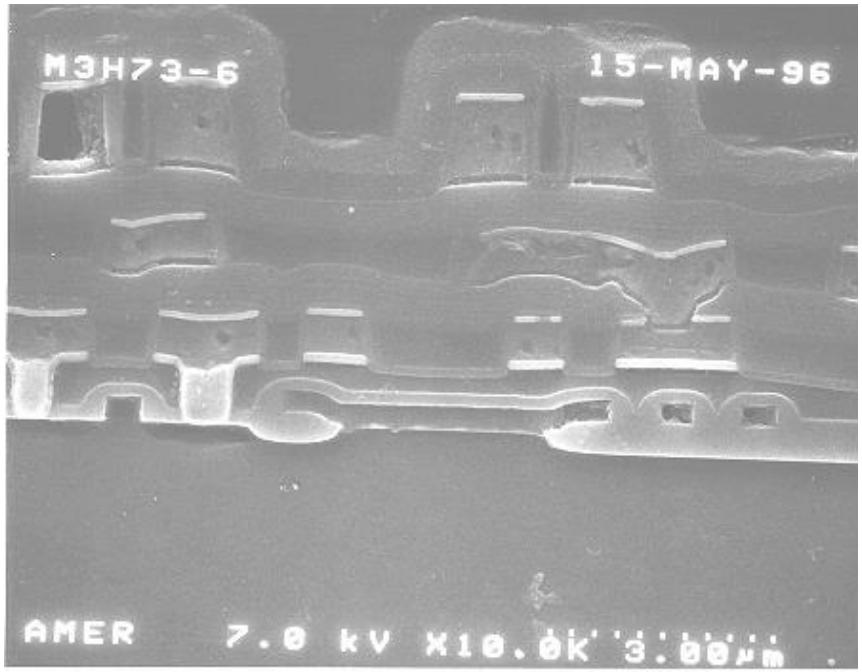


# Sección transversal A-A’

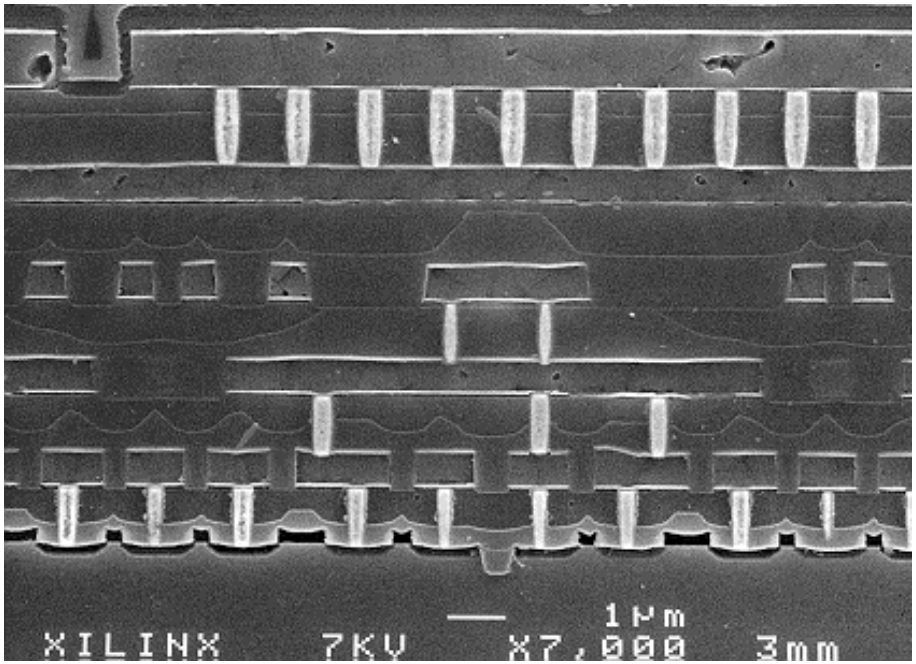


# Seccion Transversal




0.5u Process




0.25u UMC Process

# Proceso Tecnológico CMOS


Obtención del silicio


Pulido


Corte

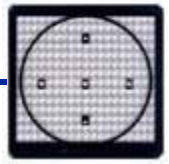

Pulido


Crecimiento Epitaxial

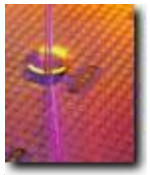

Oxidación Térmica


Aplicación de Fotoresina


Stepper


Máscara


Recocido


de Zarag
Limpieza

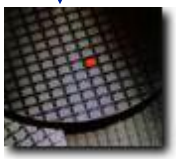

Secado


Implantación Iónica


Difusión


Implantación de Metal

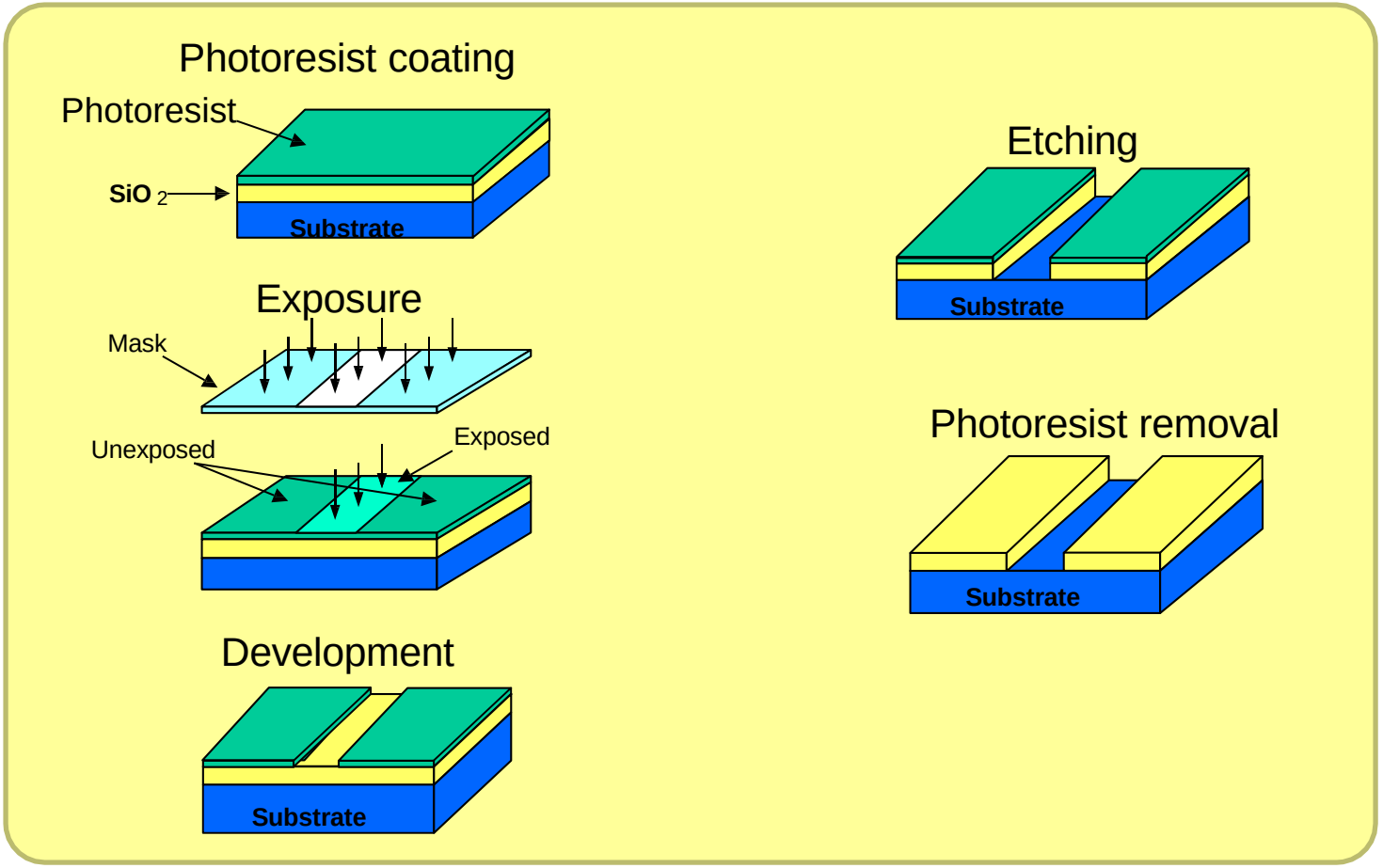

Limpieza y Pasivación


Test del circuito y Corte


Cableado

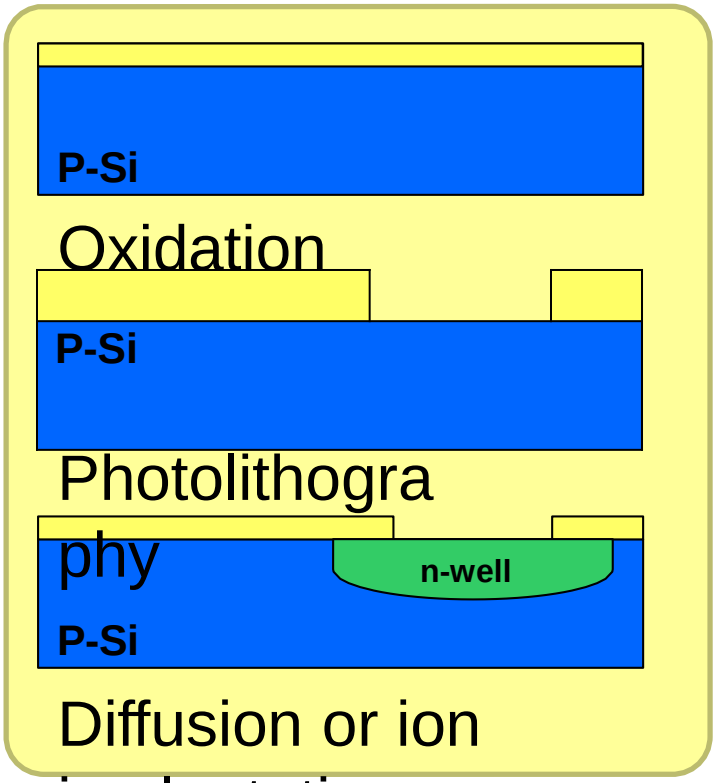

Encapsulado

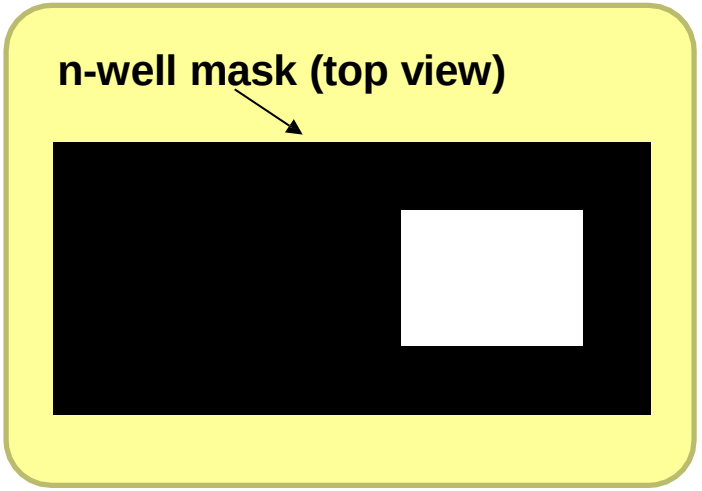
# Etapas fotolitográficas



# Ejemplo de máscaras

- N-well Process mask

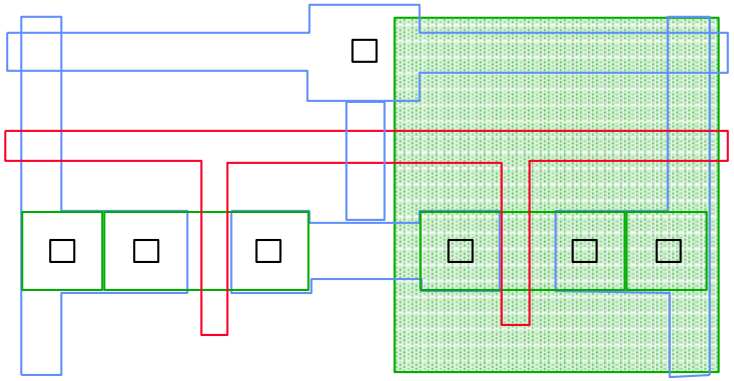


# Máscara de pozo N

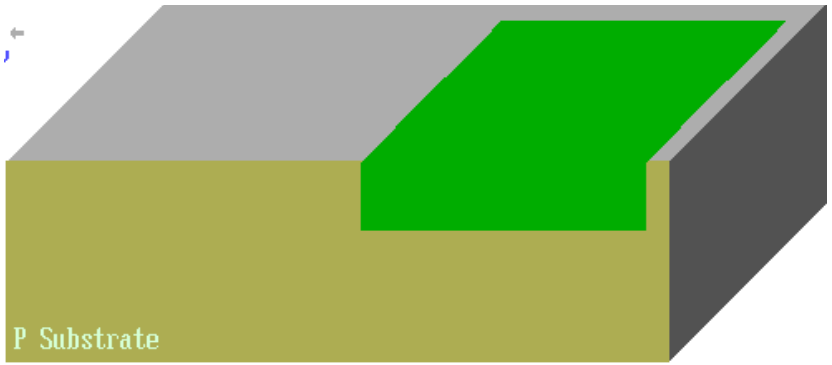
1 Difusión del Pozo N

espesor=7-10 Å



2 Recrecimiento de

óxido fino



# Máscaras de difusión N y P

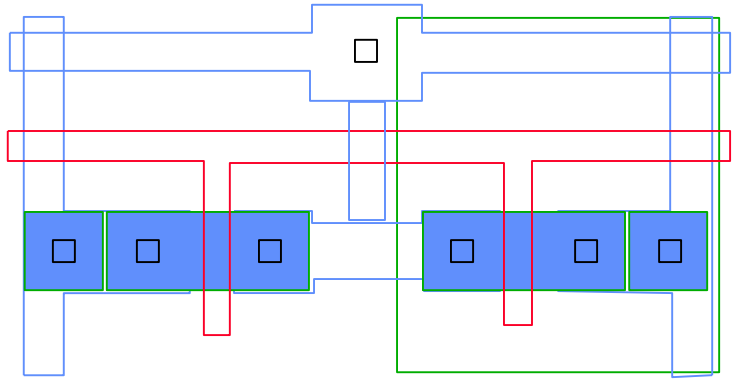
3Implantación de una barrera de $Si_3N_4$

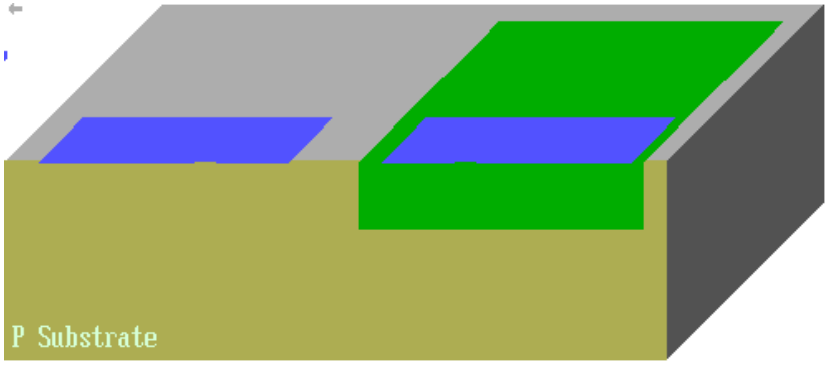
(protección de las *zonas activas*)

4Recrecimiento del óxido grueso de aislamiento

(máscara inversa)

5 Limpieza del óxido fino y el $Si_3N_4$

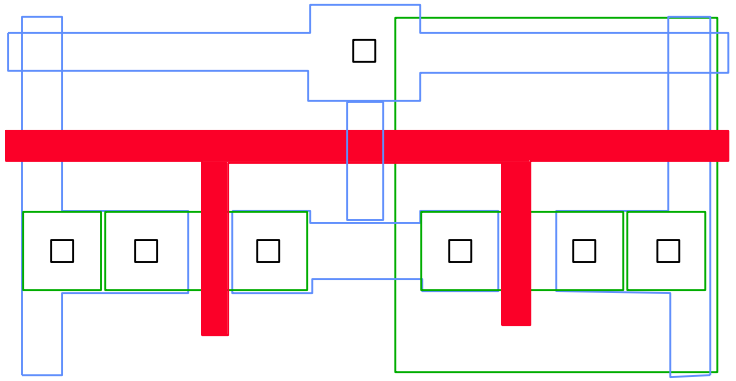




# Máscara de polisilicio

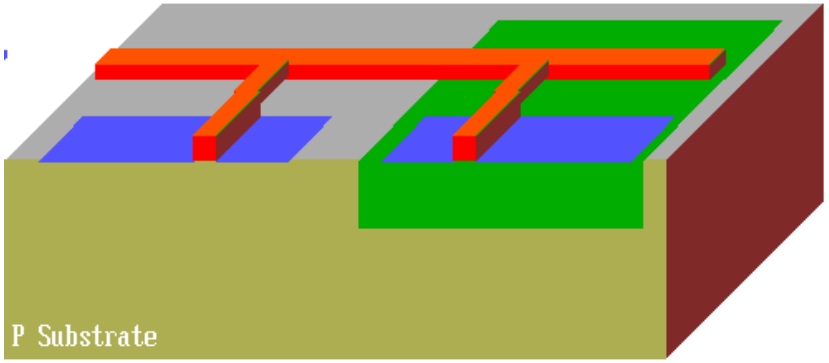
6 Recrecimiento del óxido de puerta

espesor = 350-500 Å



7 Implantación del polisilicio

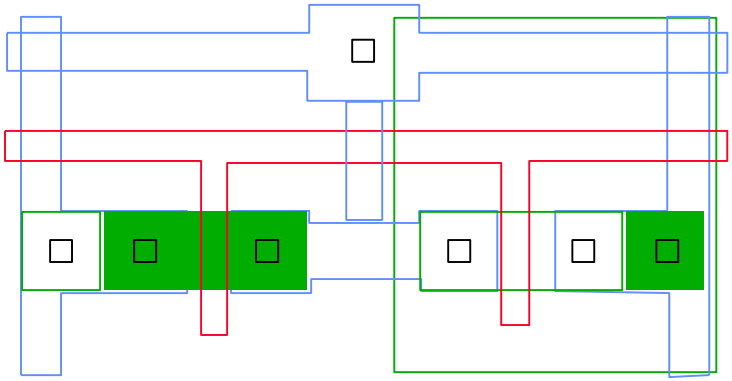
espesor = 5000-1000 Å

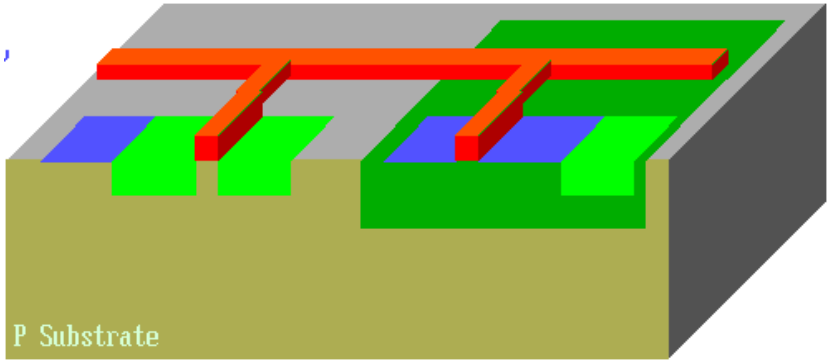


# Máscara de difusión N

8 Difusión N

espesor = 0.5-1.5 Å

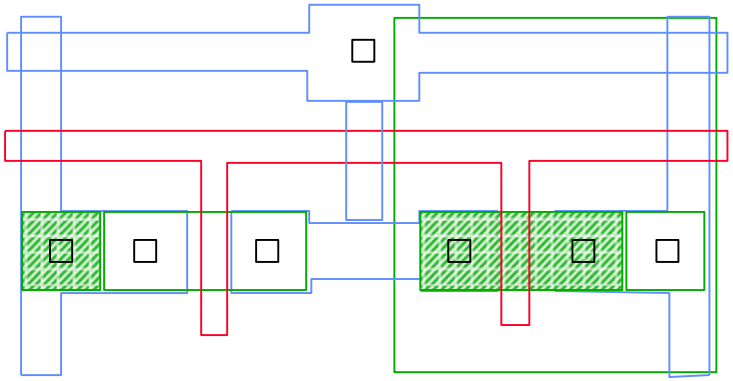




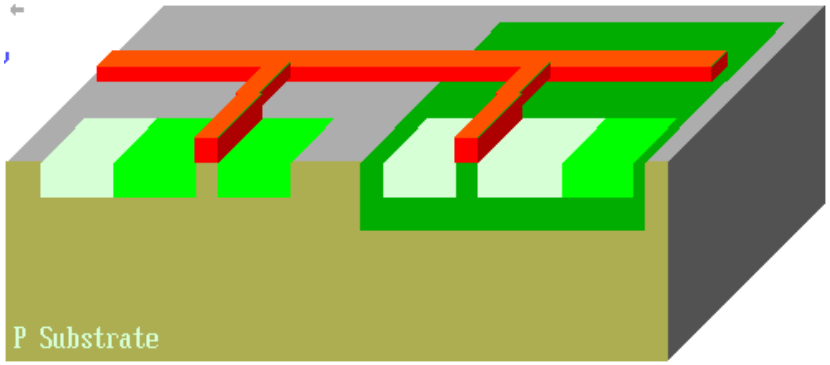
# Máscara de difusión P

9 Difusión P

espesor = 0.5-1.5 Å

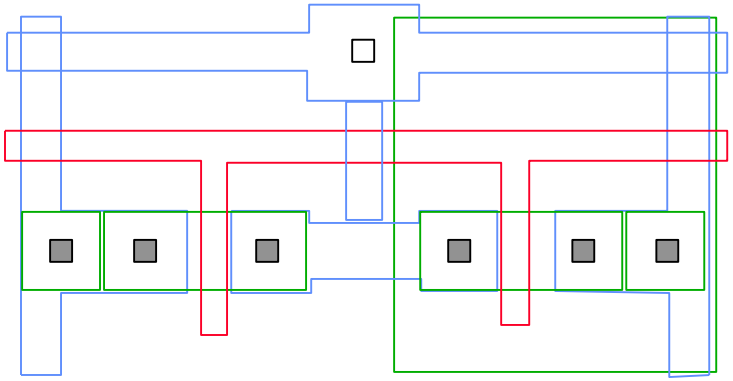


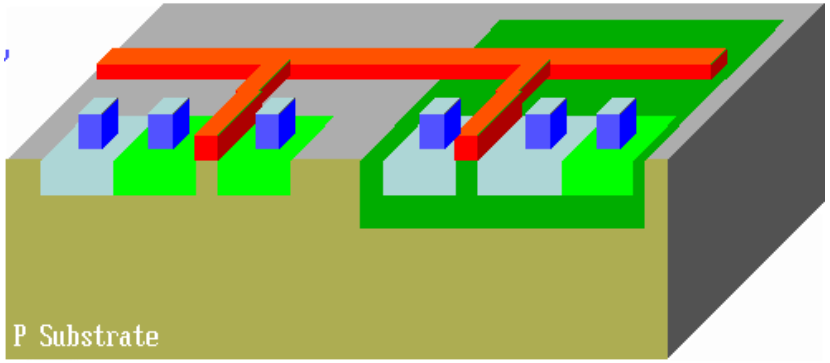
10 Deposición de $SiO_2$ en toda la oblea



# Máscara de Contactos

11 Apertura de los Contactos diff-metal_1

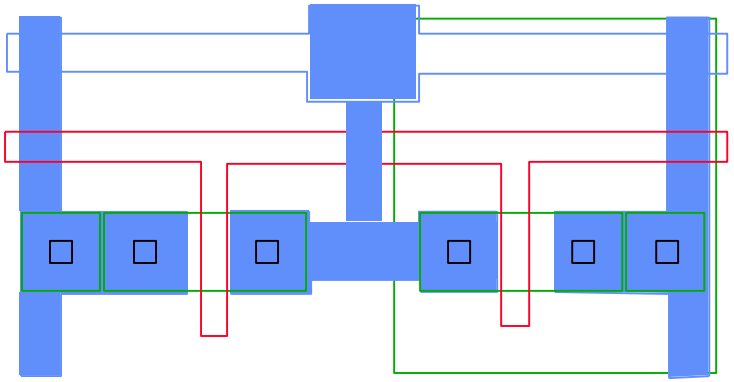




# Máscara de Metal_1

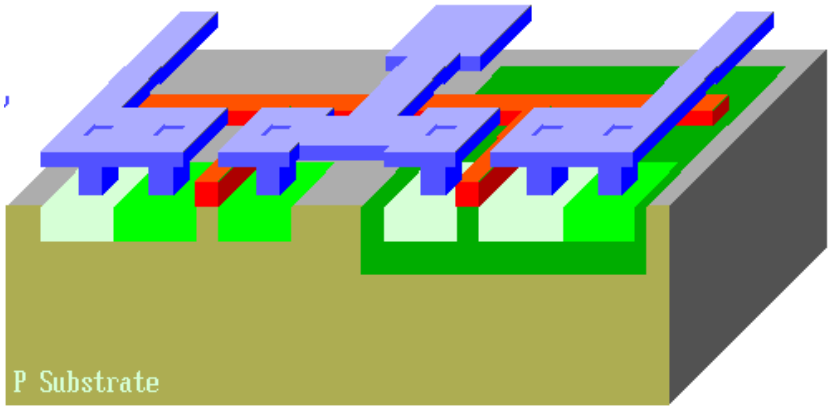
12 Metalización Metal_1

espesor = 10000 Å



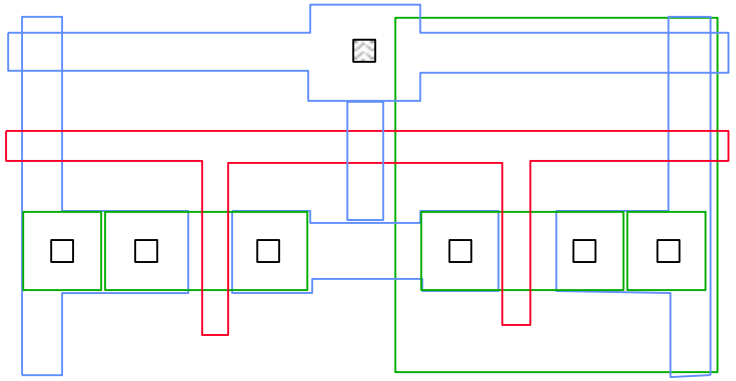
13 Deposición de $SiO_2$

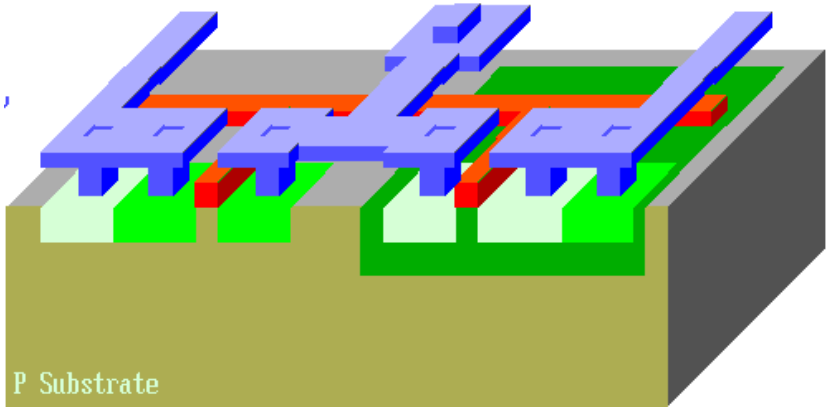
espesor = 5,000 - 10,000 Å



# Máscara de Vías

14 Apertura de las Vías
(contactos metal_1-metal_2)



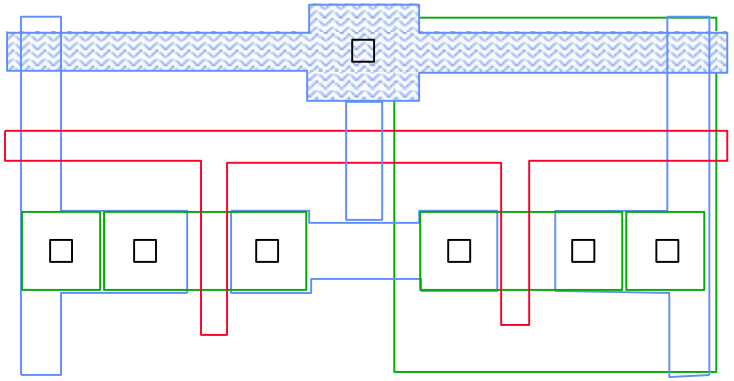


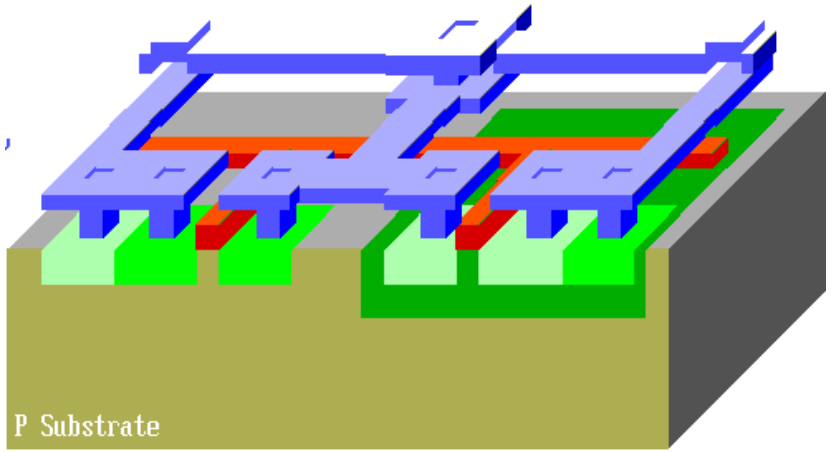
# Máscara de Metal_2

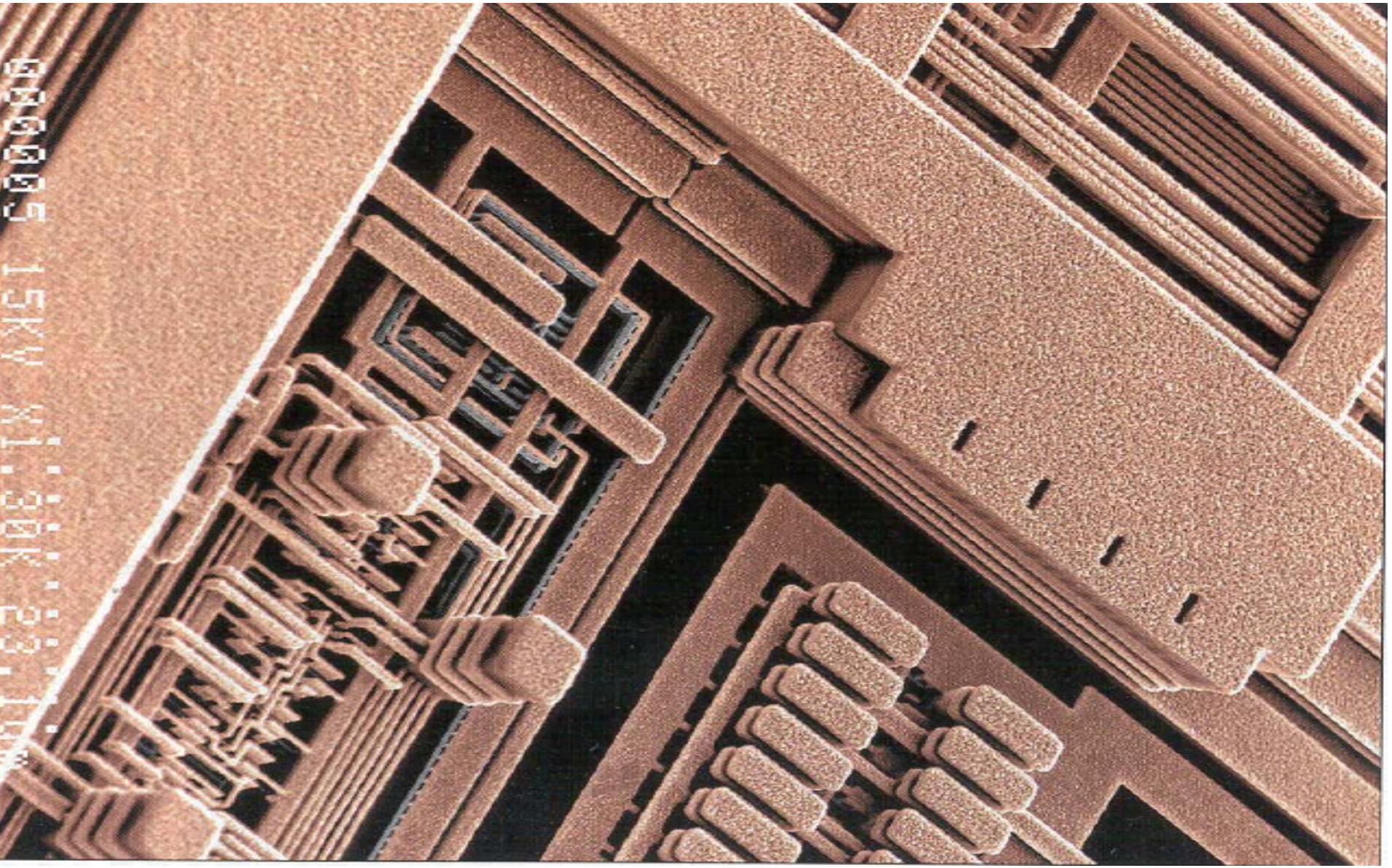
15Metalización Metal_2

espesor = 10000 Å

16Pasivación y apertura de los contactos de soldadura






000005 15kV X1,30K 23.1um

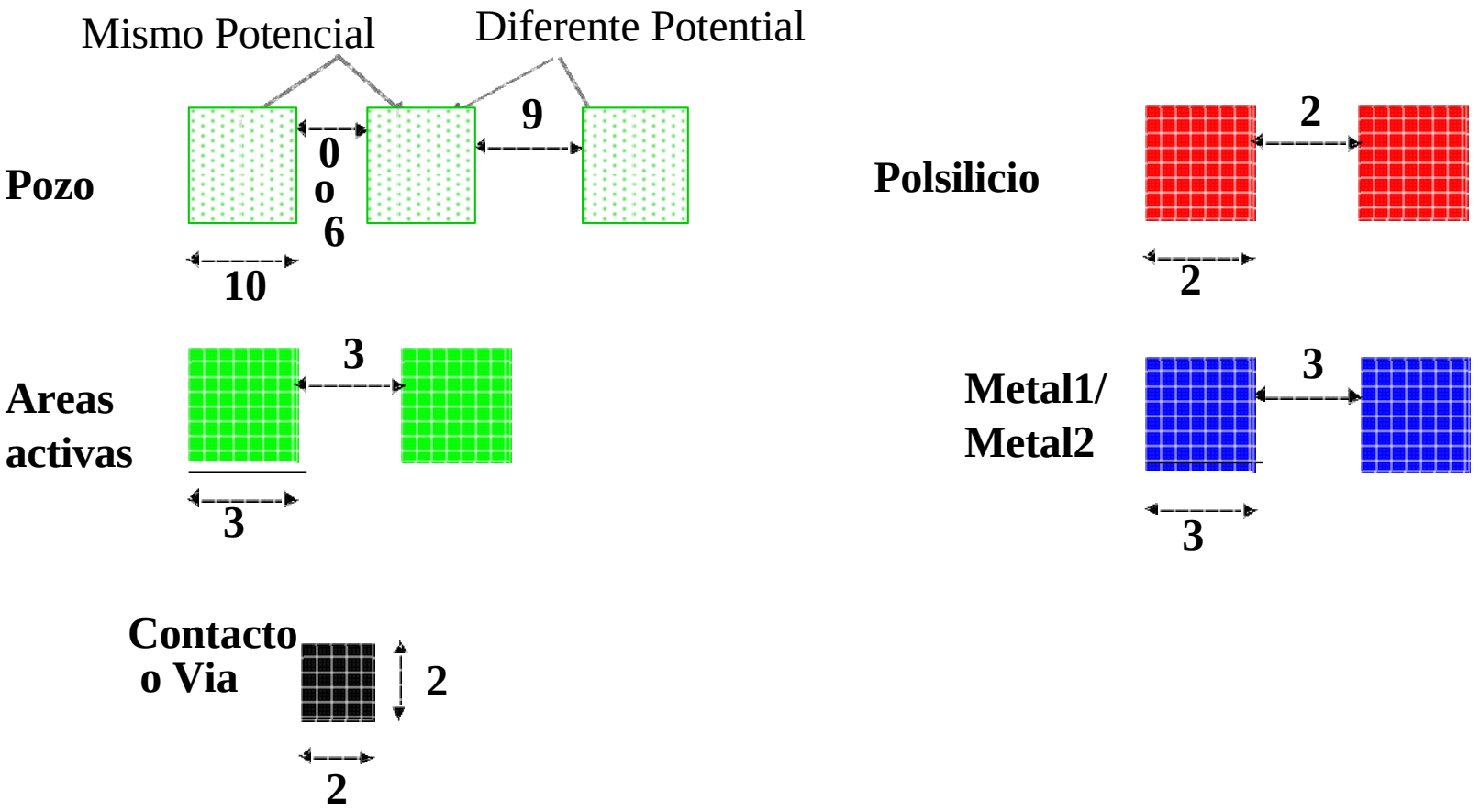
# GLOBAL FOUNDRY

https://www.youtube.com/watch?v=UvluuAIiA50

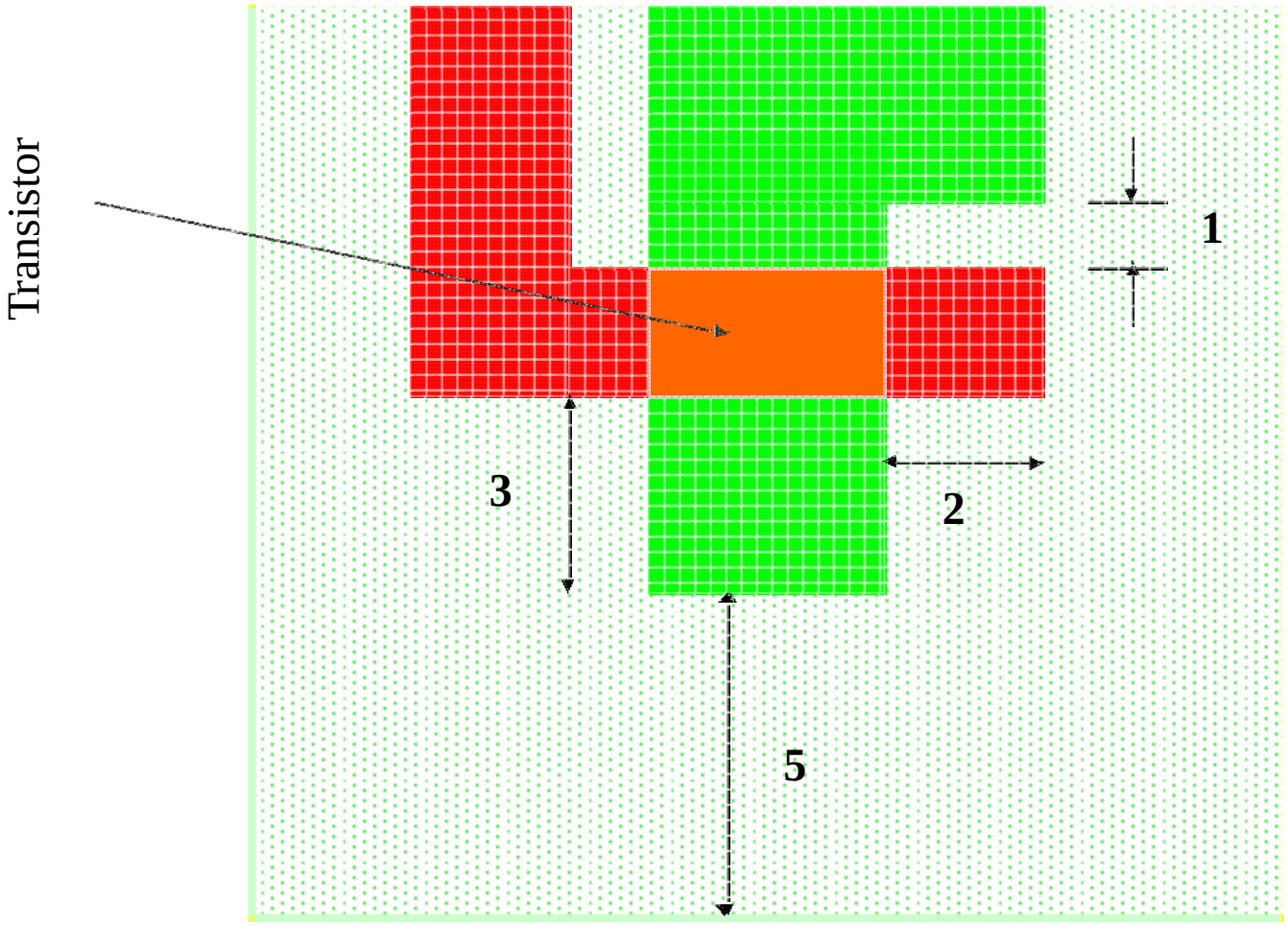
# Reglas de diseño

- Interfase entre el diseñador y el ingeniero de proceso
- Guías para construir las máscaras del proceso
- Unidades: Anchura mínima de un línea
  - Reglas escalables: parámetro lambda
  - Dimensiones absolutas

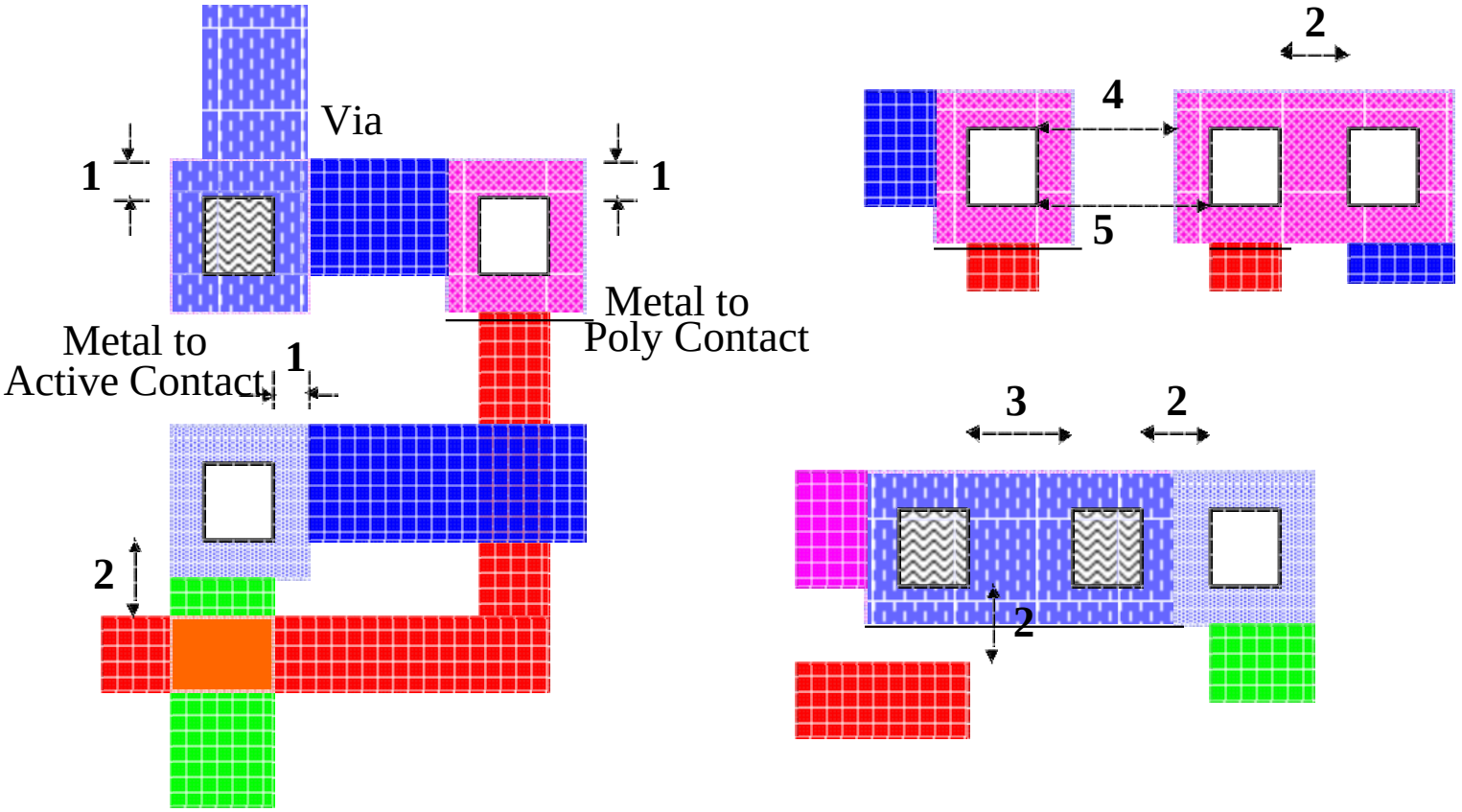
# Reglas Intra-Layer



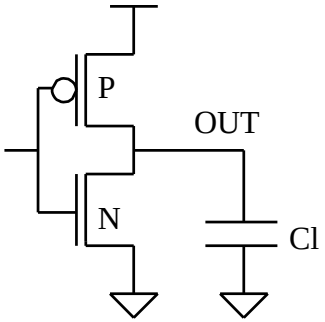
# Layout del transistor



# Vías y Contactos

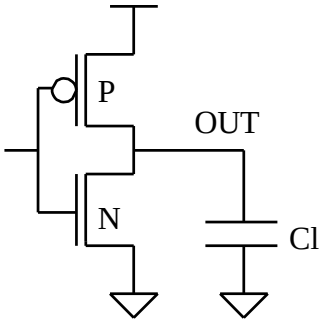


# Lógica combinacional CMOS

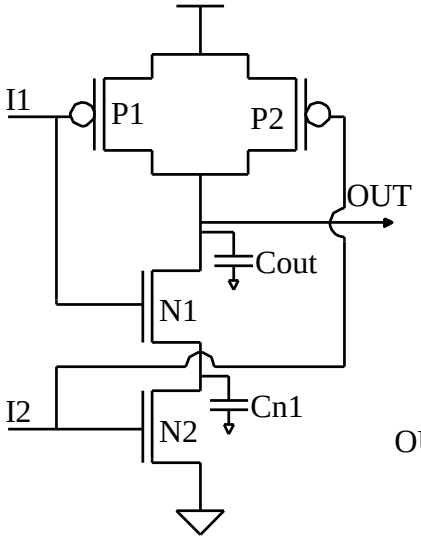



$OUT = \overline{I}$

# Lógica combinacional CMOS

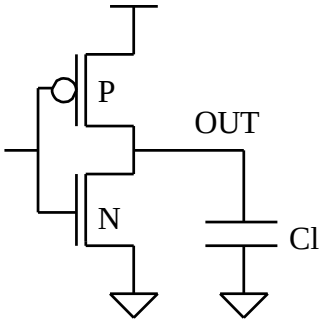



$OUT = \overline{I}$

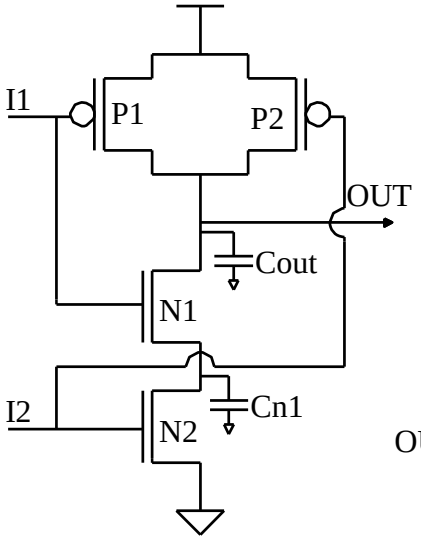



$OUT = \overline{I1*I2}$

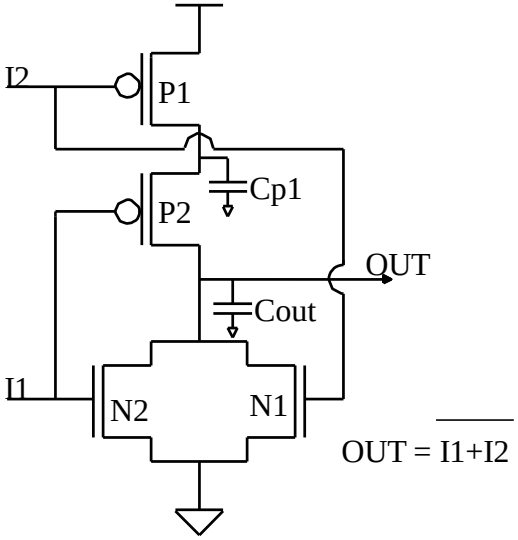
# Lógica combinacional CMOS




$OUT = \overline{I}$

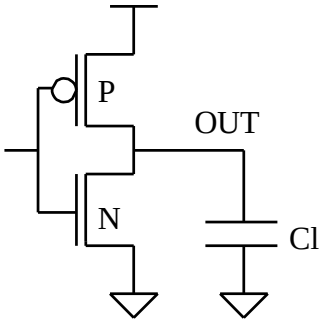



$OUT = \overline{I1 * I2}$

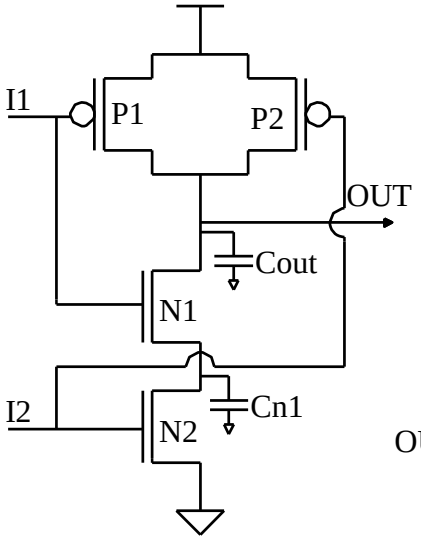



$OUT = \overline{I1 + I2}$

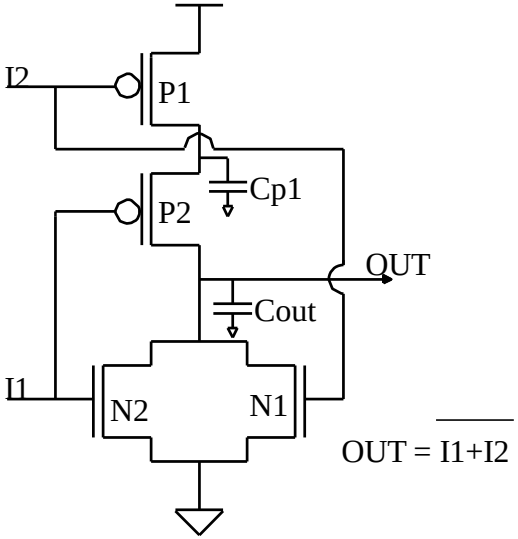
# Lógica combinacional CMOS



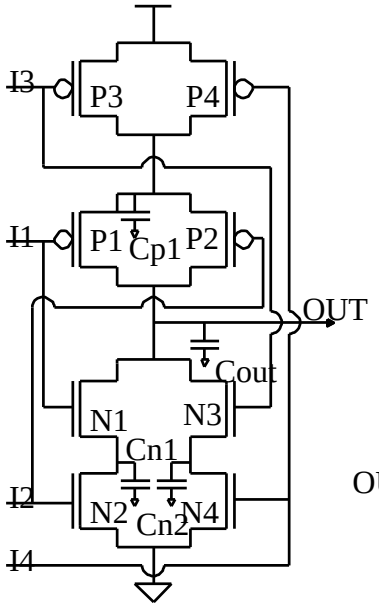

$OUT = \overline{I}$




$OUT = \overline{I1*I2}$

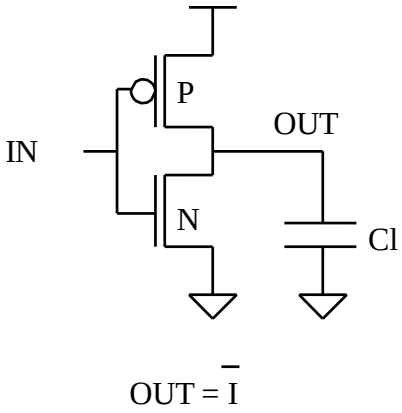


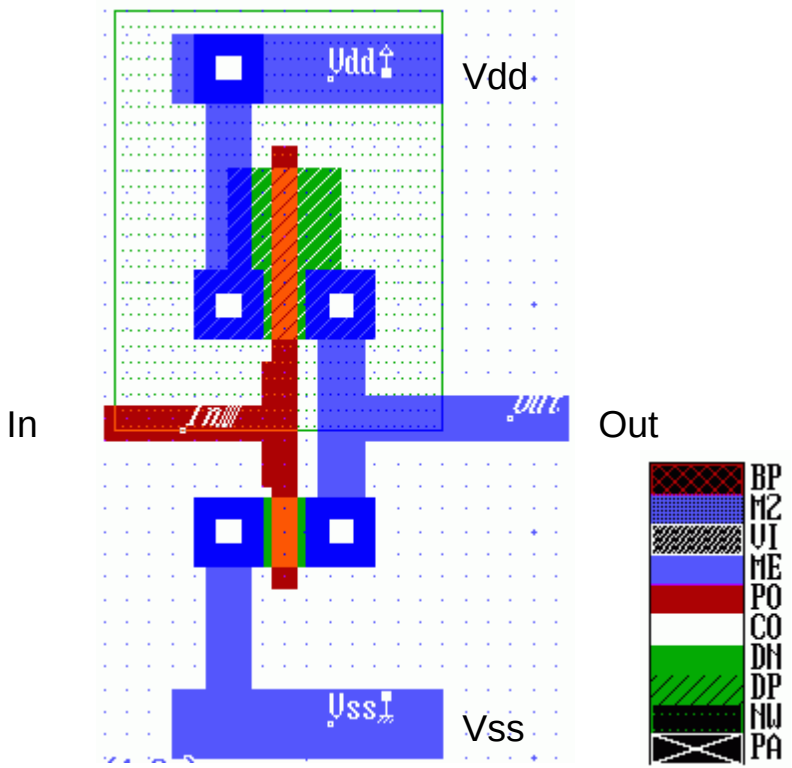

$OUT = \overline{I1+I2}$



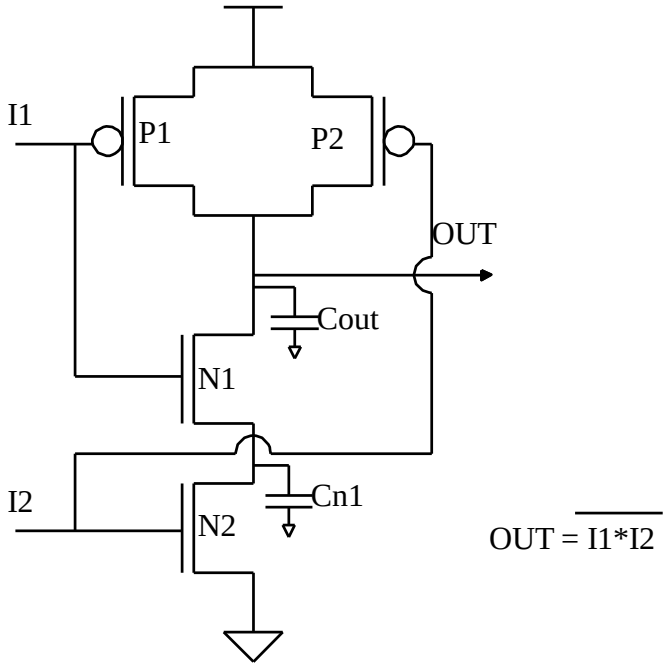

$OUT = \overline{I1*I2+I3*I4}$

# Layout CMOS: INV

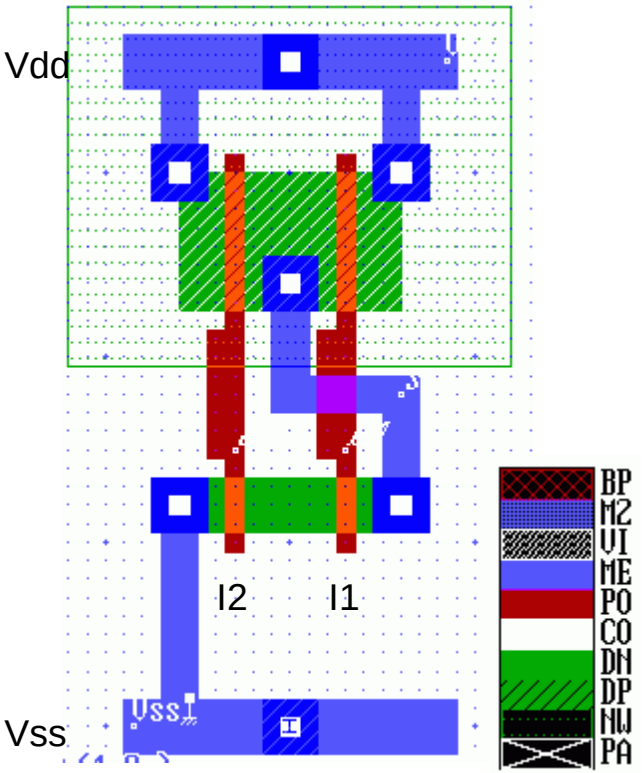


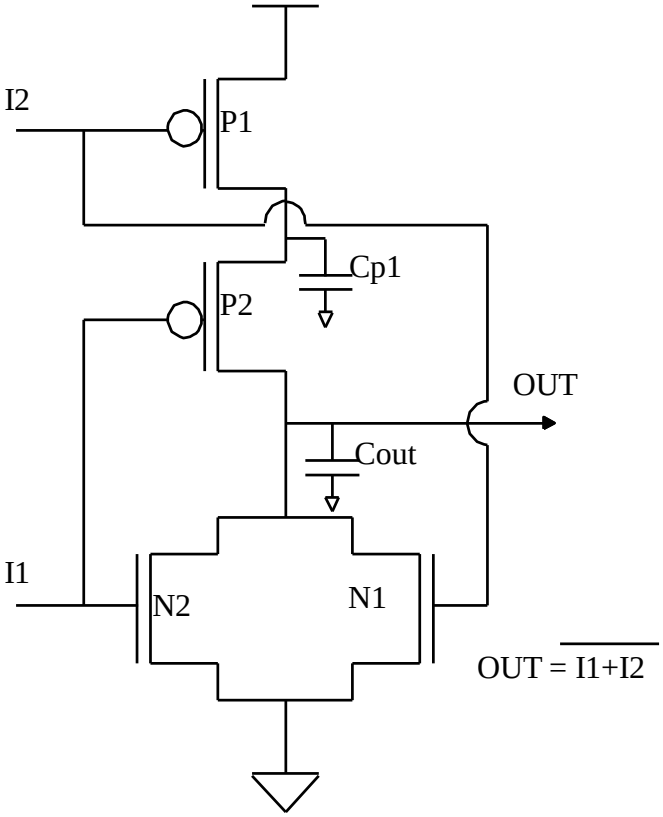
# Layout CMOS: NAND2

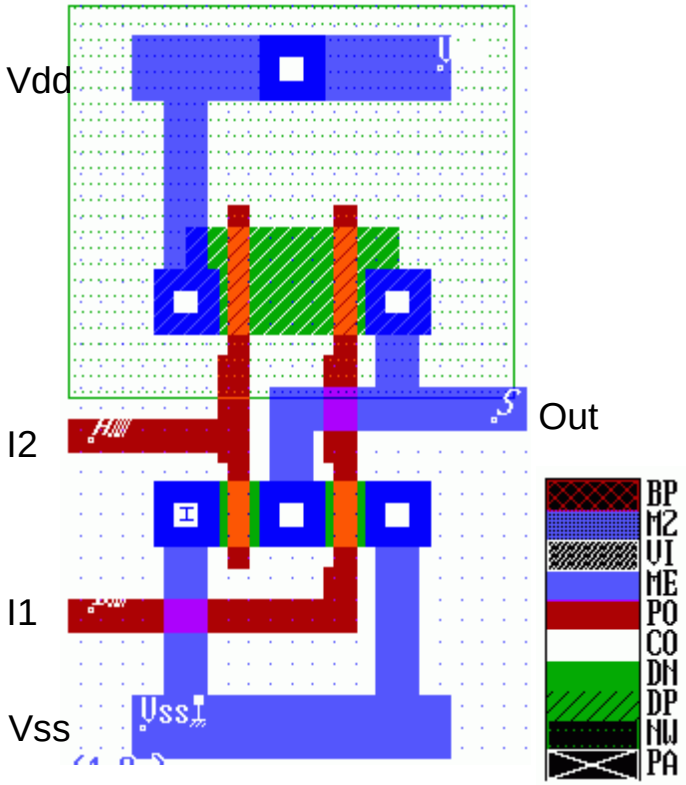



$$OUT = \overline{I1*I2}$$

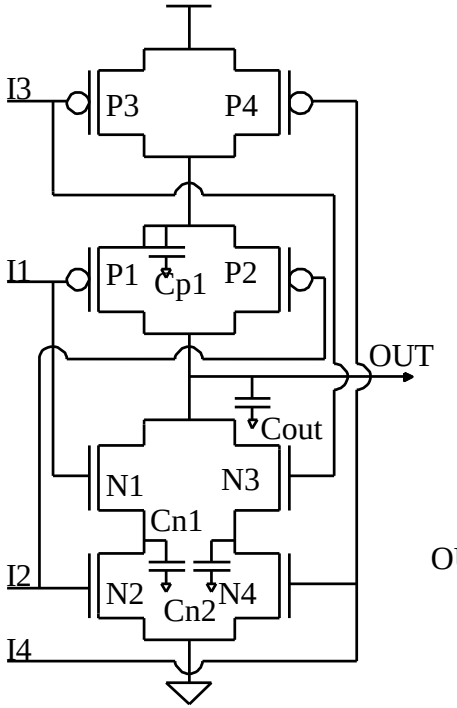


# Layout CMOS: NOR2

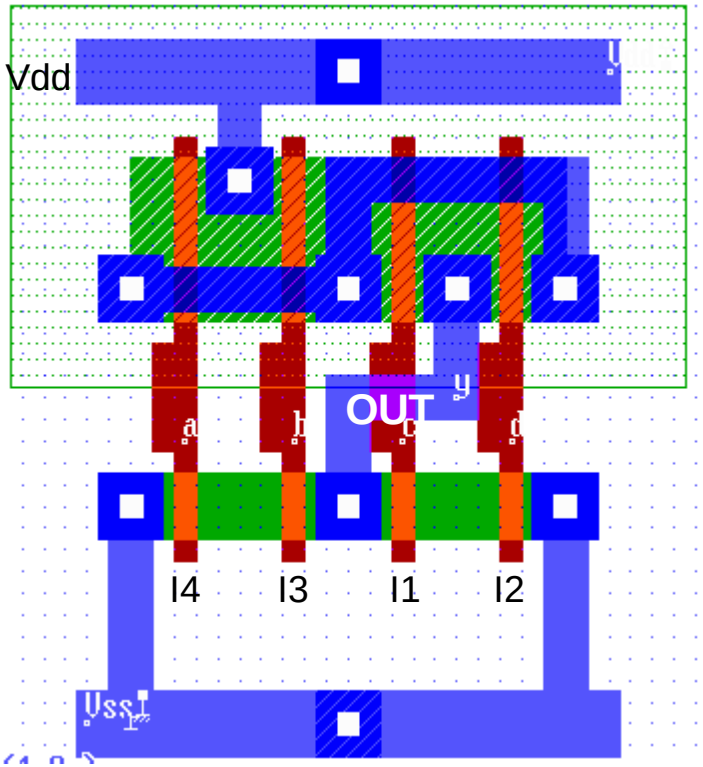


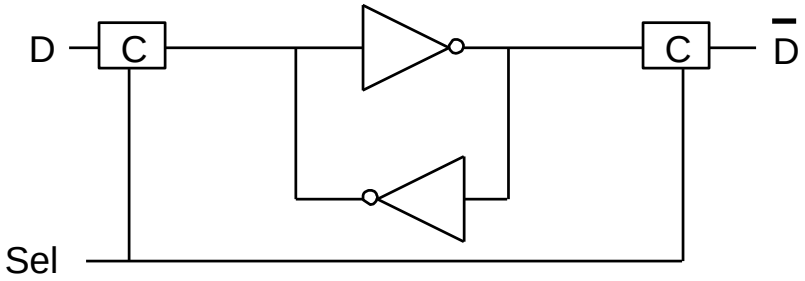
# Layout CMOS: AOI

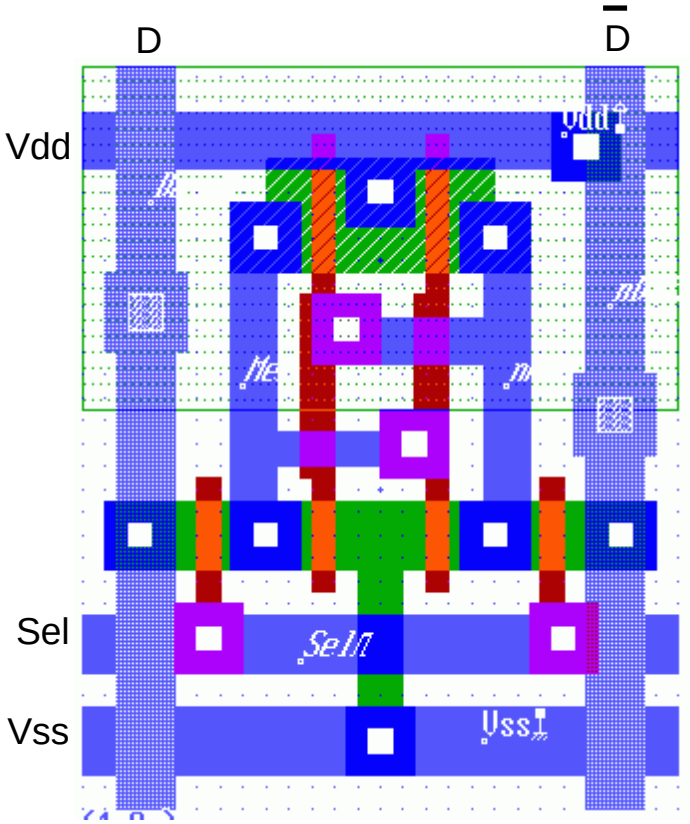



$$OUT = \overline{I1*I2+I3*I4}$$

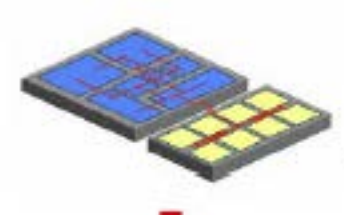


# Layout CMOS: Celda RAM

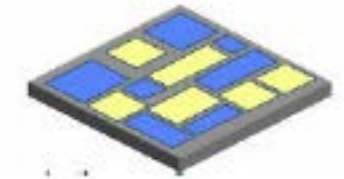


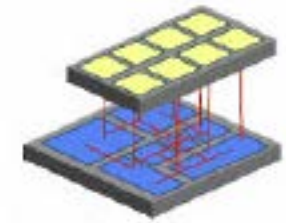
# Integración 3D



2D Interconnect



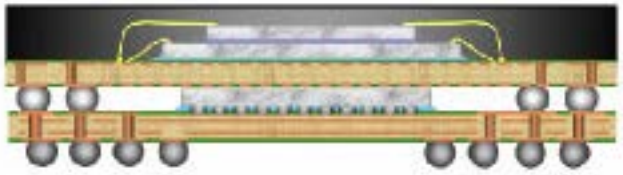
SOC Solution



3D Interconnect

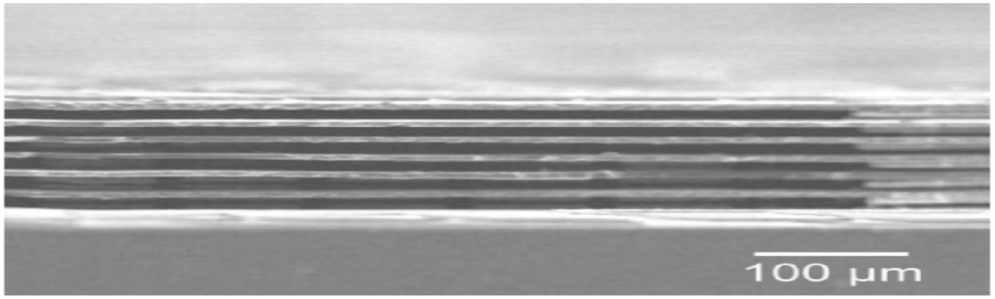
ASTRI Proprietary

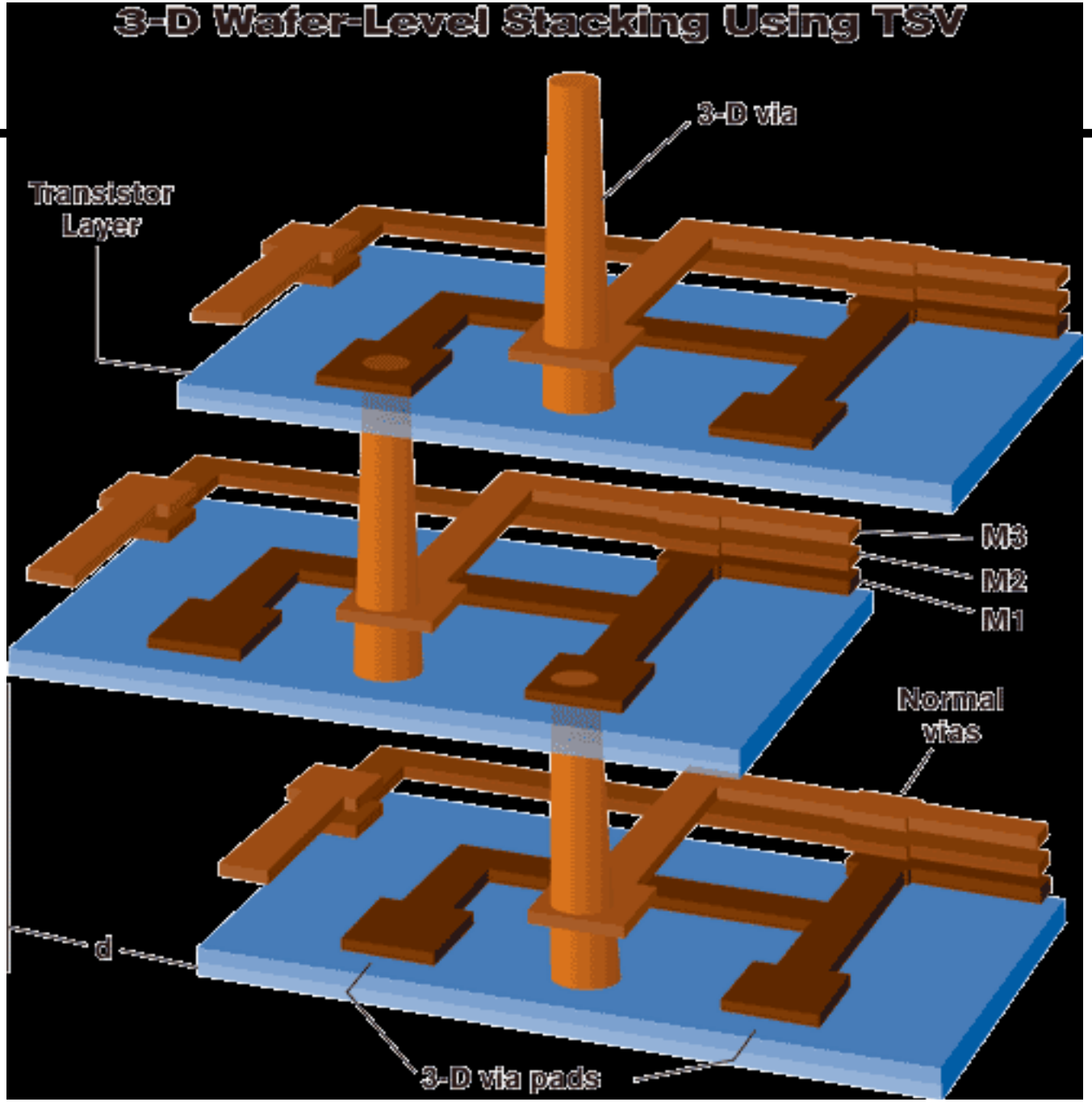
Die Stacking



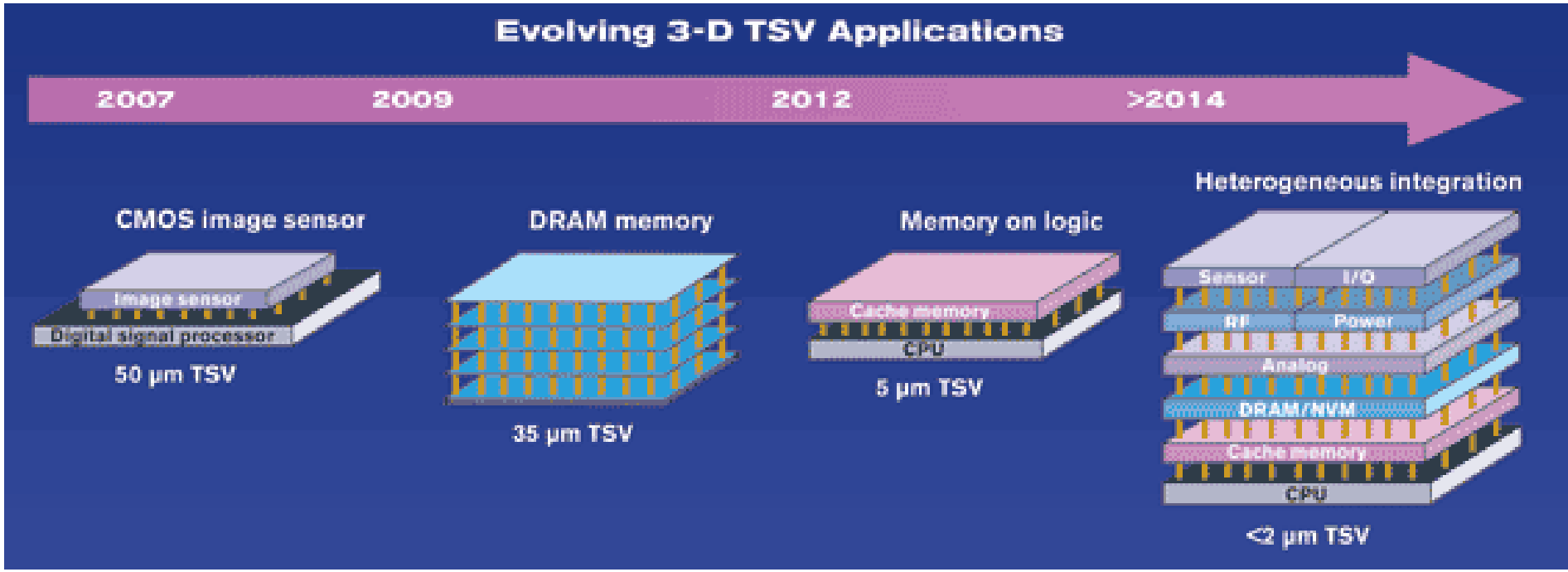
Package-on-Package (PoP)

Through Silicon Via (TSV)




3-D Wafer-Level Stacking Using TSV
3-D via
Transistor Layer
M3
M2
M1
Normal vias
d
3-D via pads

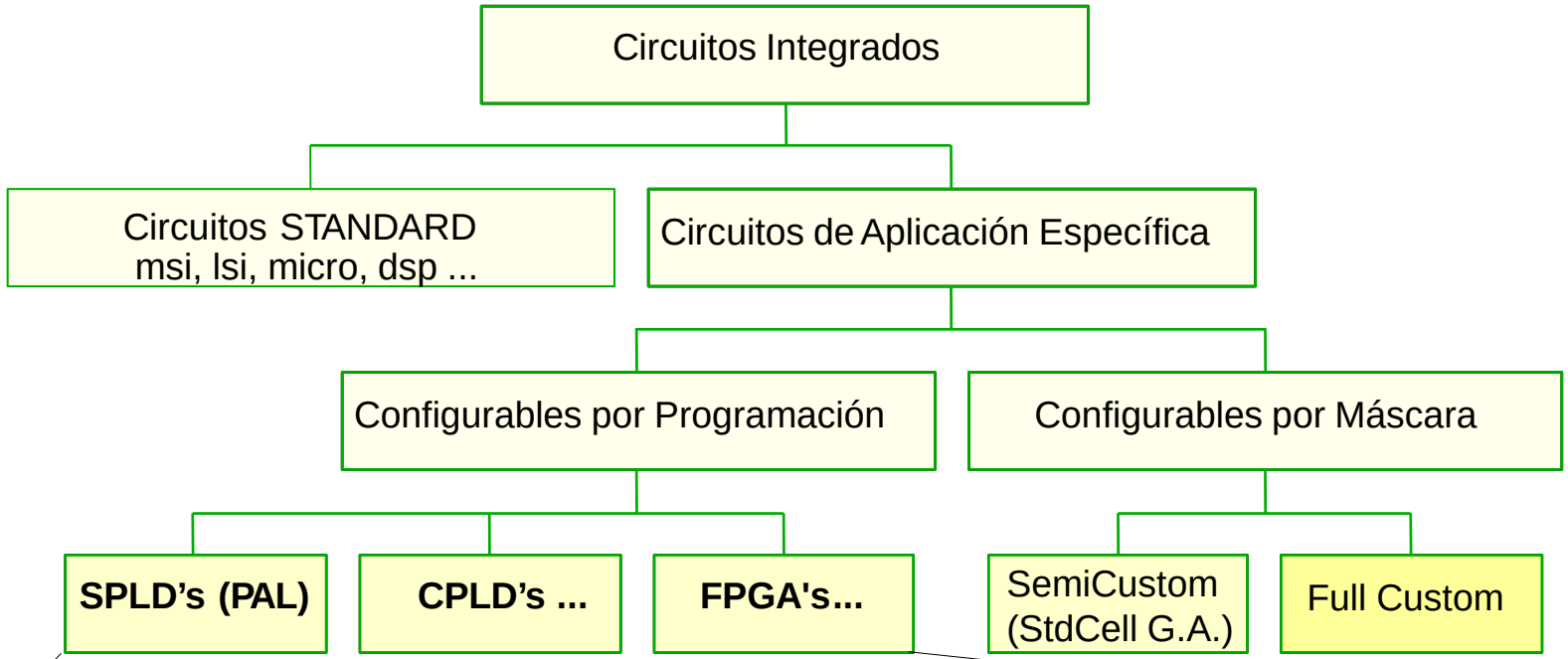
# Integración 3D



# Implementación de Sistemas Electrónicos

- Un poco de historia, evolución tecnológica
- Fabricación y diseño de C.I CMOS.
- Opciones de diseño
- Flujo de Diseño

# Opciones de Diseño



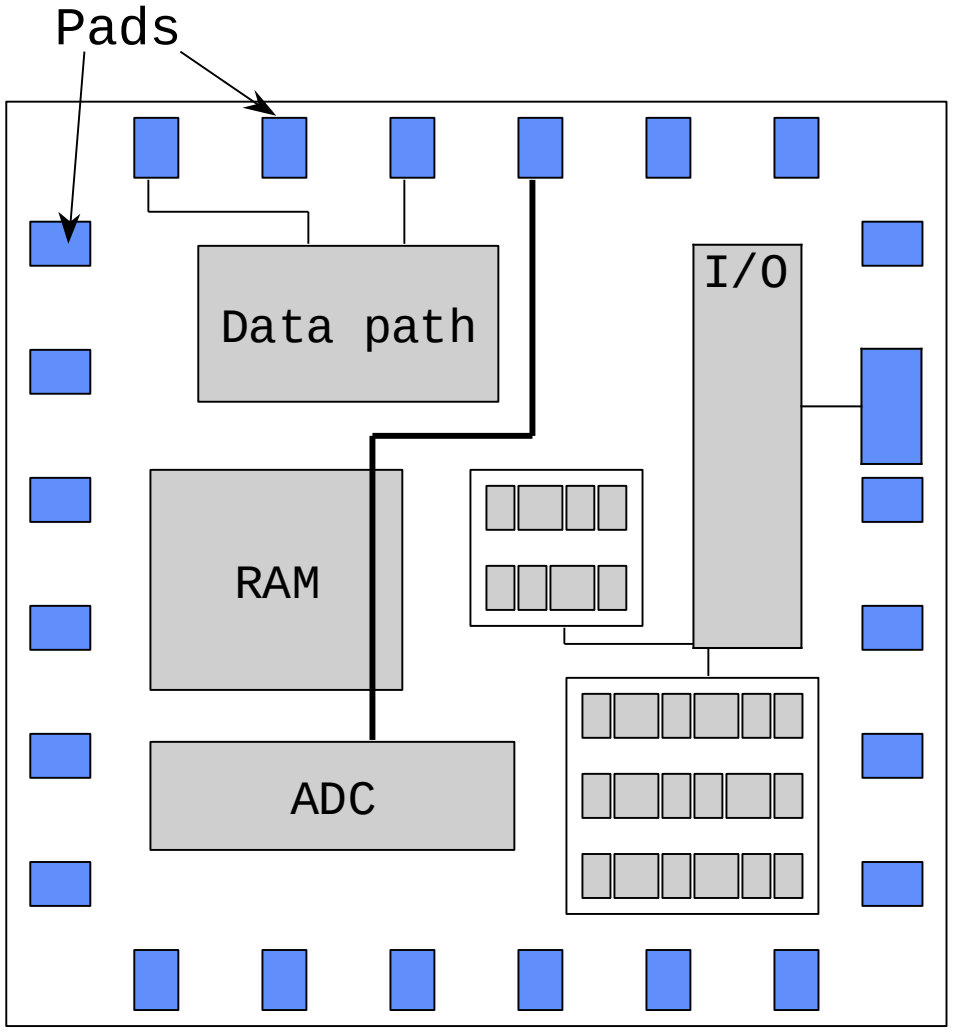

**Acrónimos**

**SPLD** = Simple Prog. Logic Device
**PAL** = Prog. Array of Logic
**CPLD** = Complex PLD
**FPGA** = Field Prog. Gate Array

**Recursos**

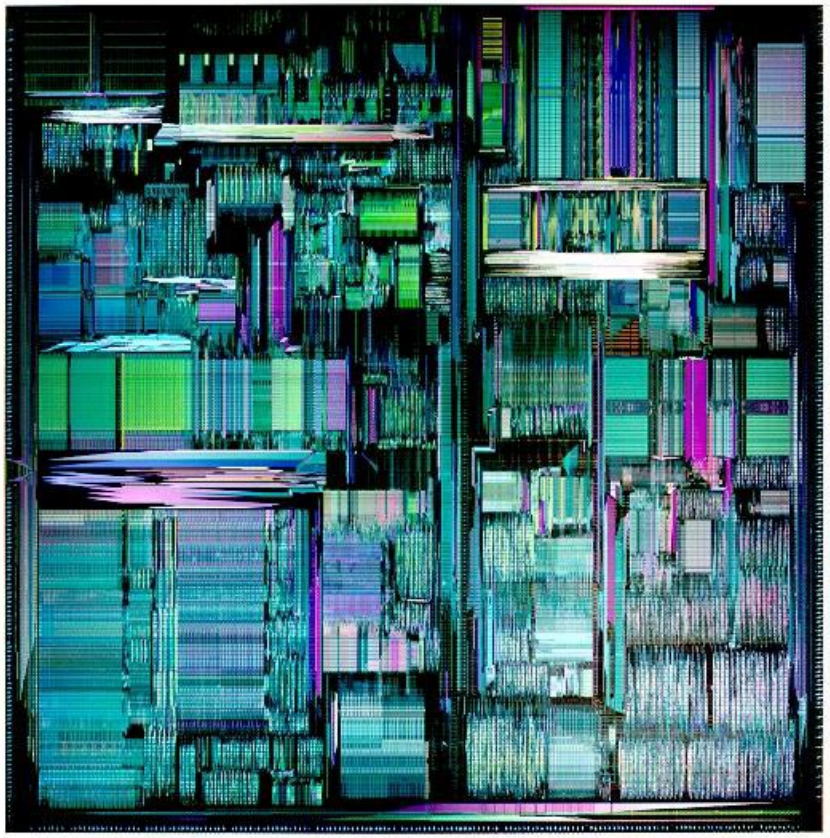
Configurable Logic Blocks (CLB): Memory Look-Up Table
Planos AND-OR
Puertas lógicas
Input / Output Blocks (IOB)
Bidirecional, latches, inversores, pullup/pulldowns
Interconexión or Routing
Local, realimentación interna, global

# Estructura Full-Custom

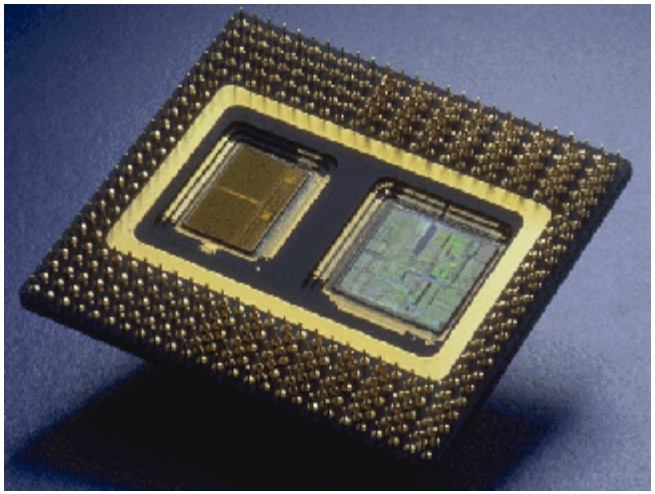


# Pentiun Pro (P6) 1995

Microprocesador

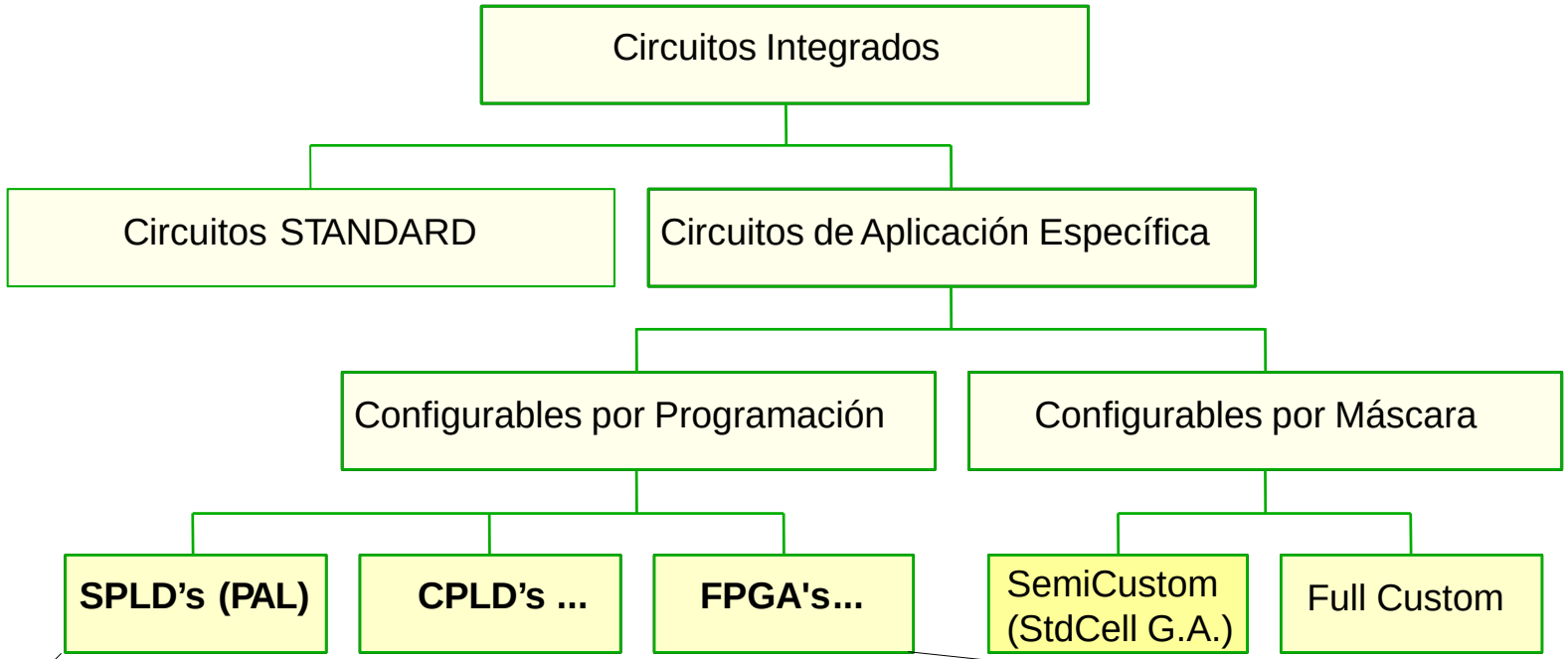


Multi Chip Mudule
Microprocesador y Cache



Intel p6: 32 bits
5.5 M transistores
200 Mhz.
0.35µm, 4 metales

# Opciones de Diseño



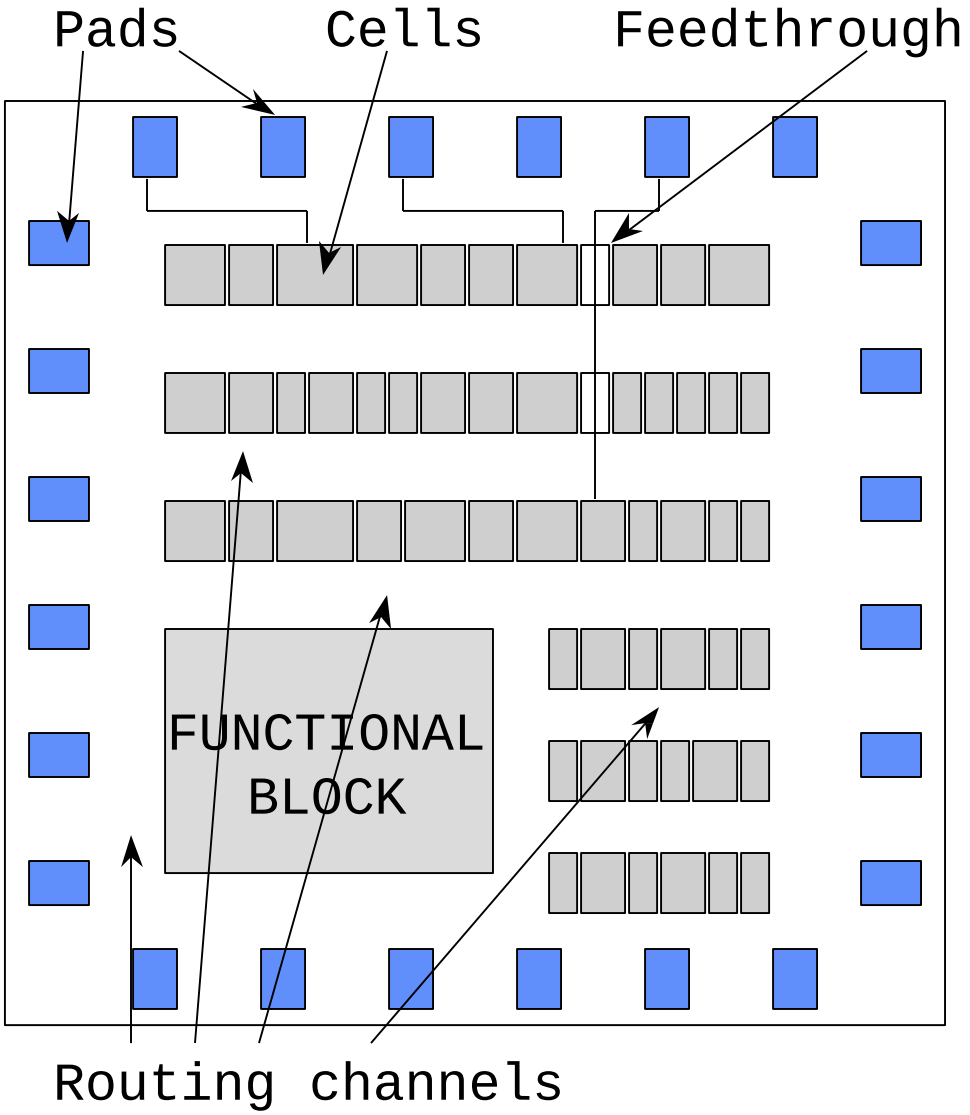

**Acrónimos**

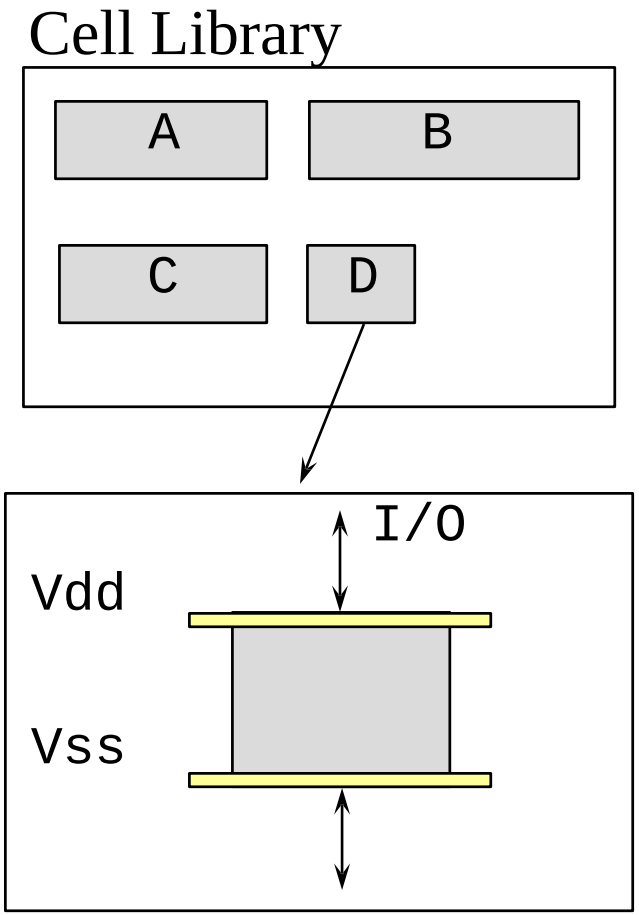
**SPLD** = Simple Prog. Logic Device
**PAL** = Prog. Array of Logic
**CPLD** = Complex PLD
**FPGA** = Field Prog. Gate Array

**Recursos**

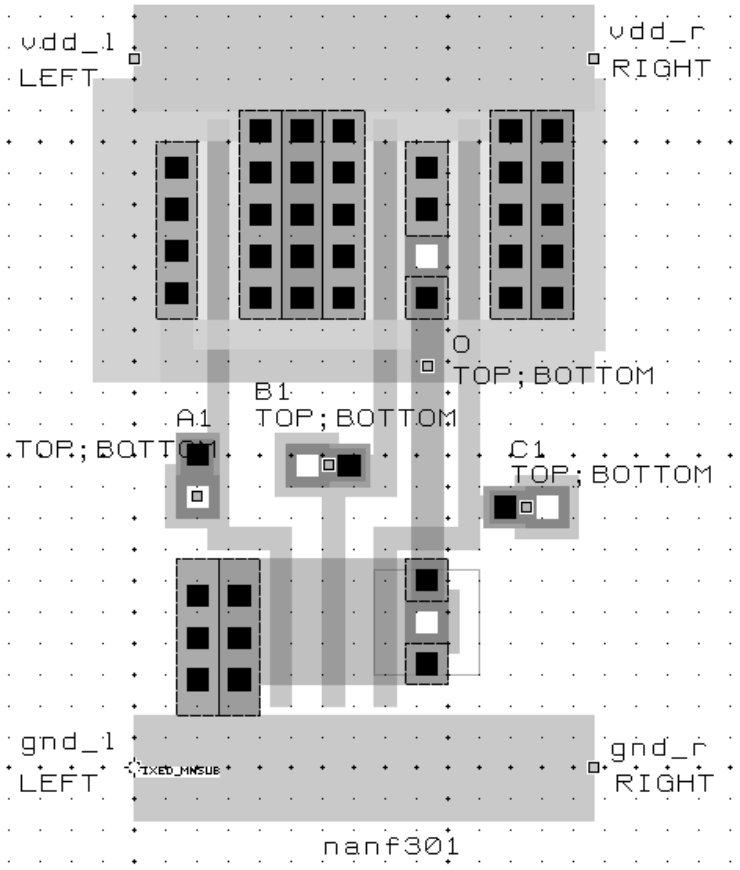
Configurable Logic Blocks (CLB): Memory Look-Up Table
Planos AND-OR
Puertas lógicas
Input / Output Blocks (IOB)
Bidirecional, latches, inversores, pullup/pulldowns
Interconexión or Routing
Local, realimentación interna, global

# Estructura Standard Cell



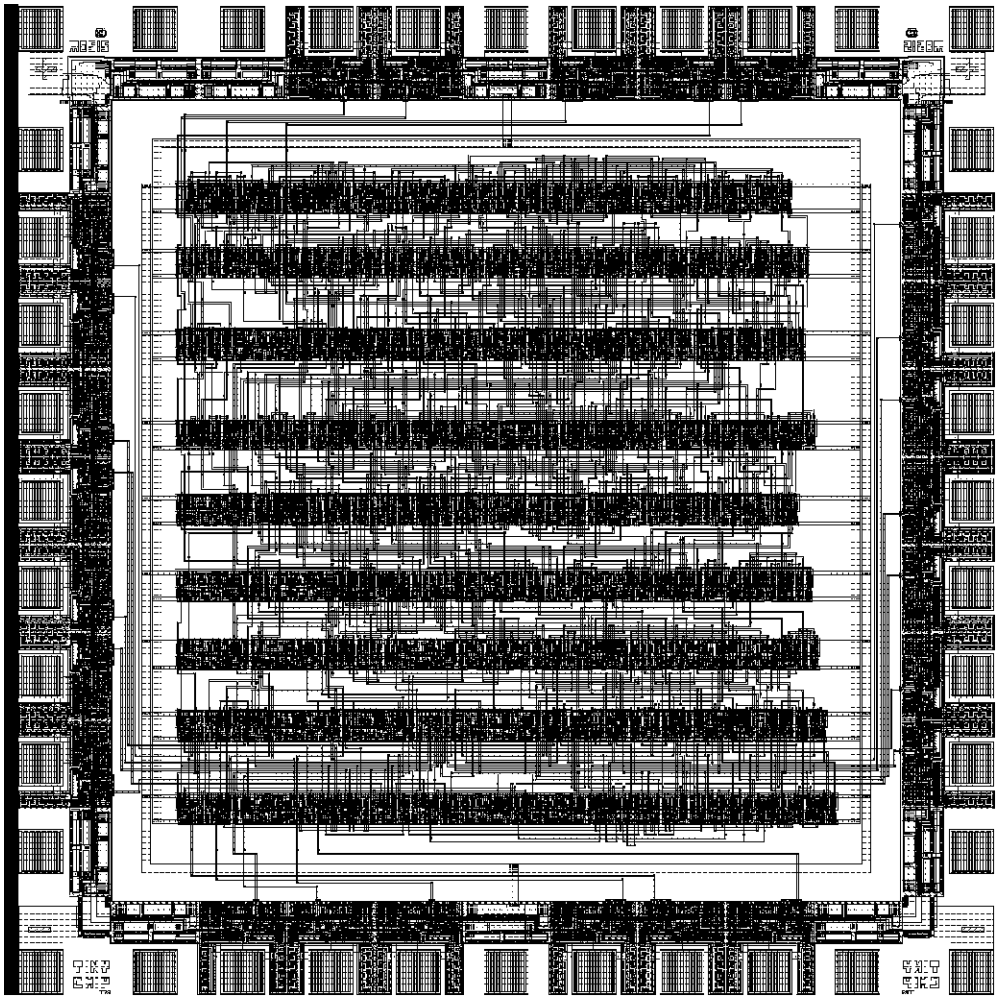
# Standard Cell




| Fanout 4x | 0.5 μm | 1.0 μm | 2.0 μm |
|---|---|---|---|
| *A1_tphl* | 0.595 | 0.711 | 0.919 |
| *A1_tplh* | 0.692 | 0.933 | 1.360 |
| *B1_tphl* | 0.591 | 0.739 | 1.006 |
| *B1_tplh* | 0.620 | 0.825 | 1.1.81 |
| *C1_tphl* | 0.574 | 0.740 | 1.029 |
| *C1_tplh* | 0.554 | 0.728 | 1.026 |

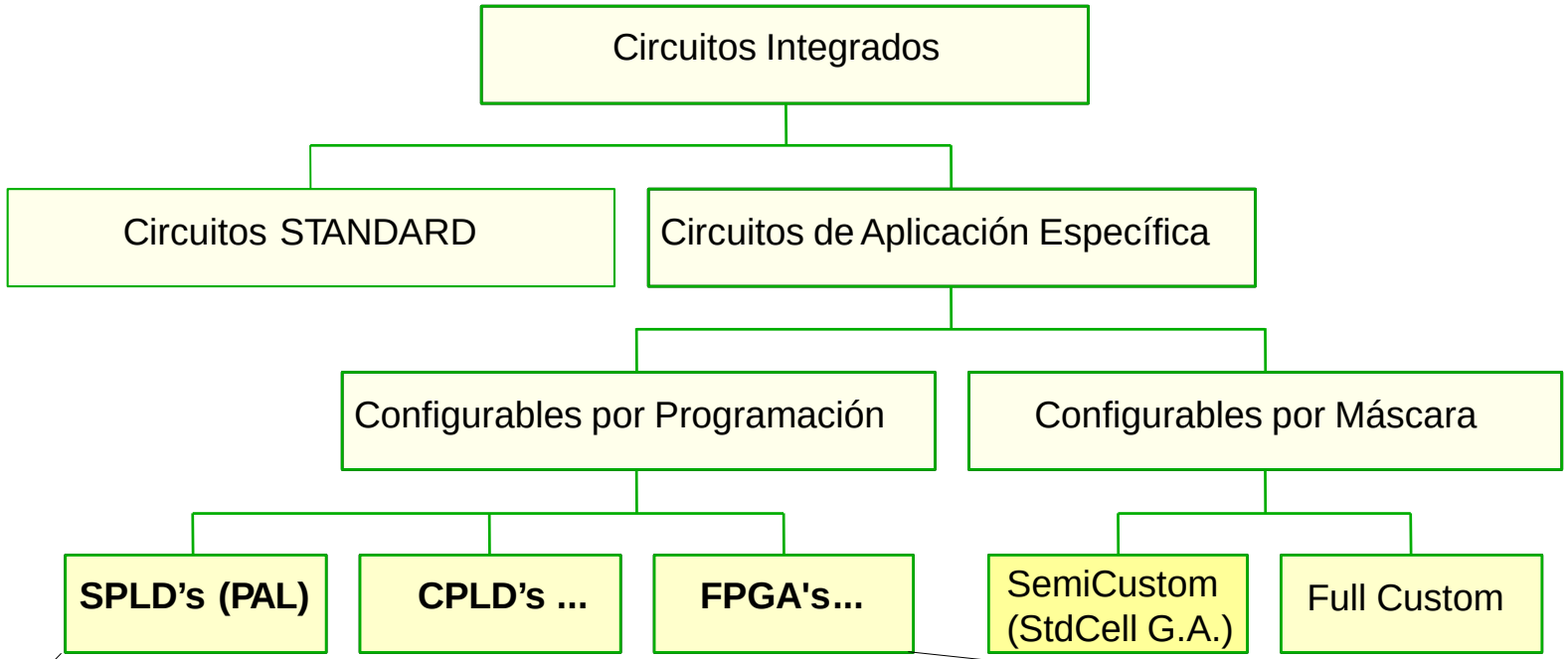
3-input NAND cell
(from Mississippi State Library)
characterized for fanout of 4 and
for three different technologies

# Standard Cell chip



[Brodersen92]

# Opciones de Diseño



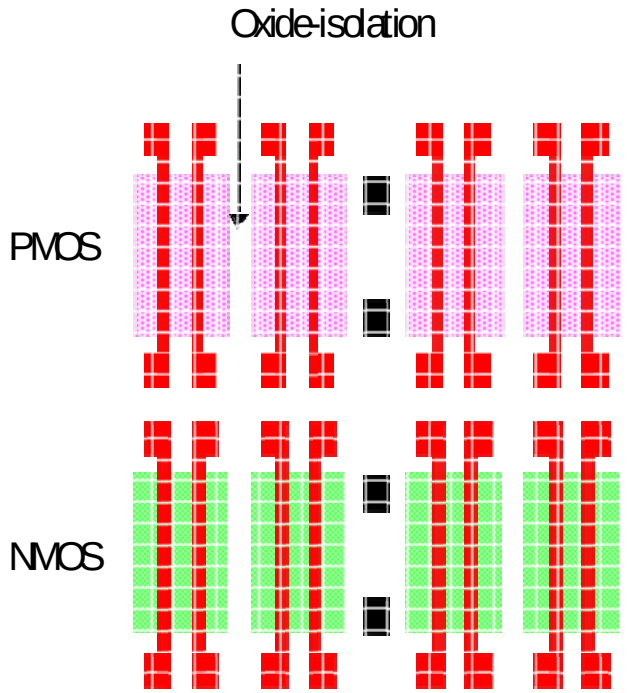

**Acrónimos**

**SPLD** = Simple Prog. Logic Device
**PAL** = Prog. Array of Logic
**CPLD** = Complex PLD
**FPGA** = Field Prog. Gate Array

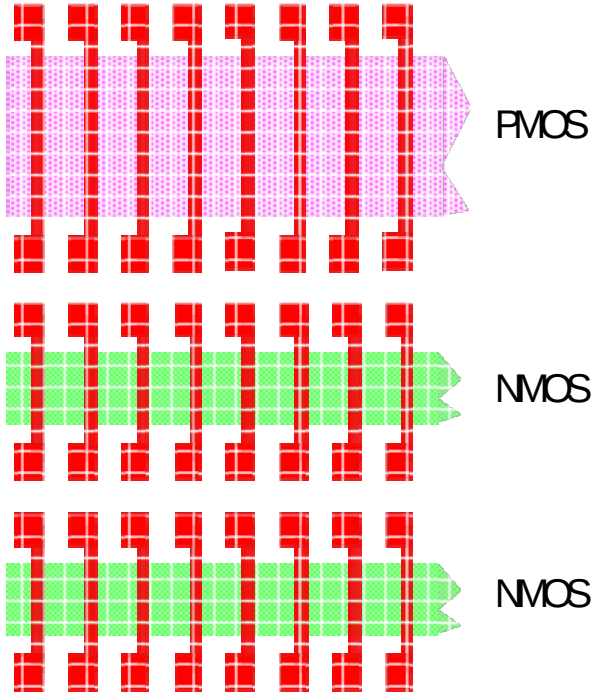
**Recursos**

Configurable Logic Blocks (CLB): Memory Look-Up Table
Planos AND-OR
Puertas lógicas
Input / Output Blocks (IOB)
Bidirecional, latches, inversores, pullup/pulldowns
Interconexión or Routing
Local, realimentación interna, global

# Sea-of-gate Primitive Cells

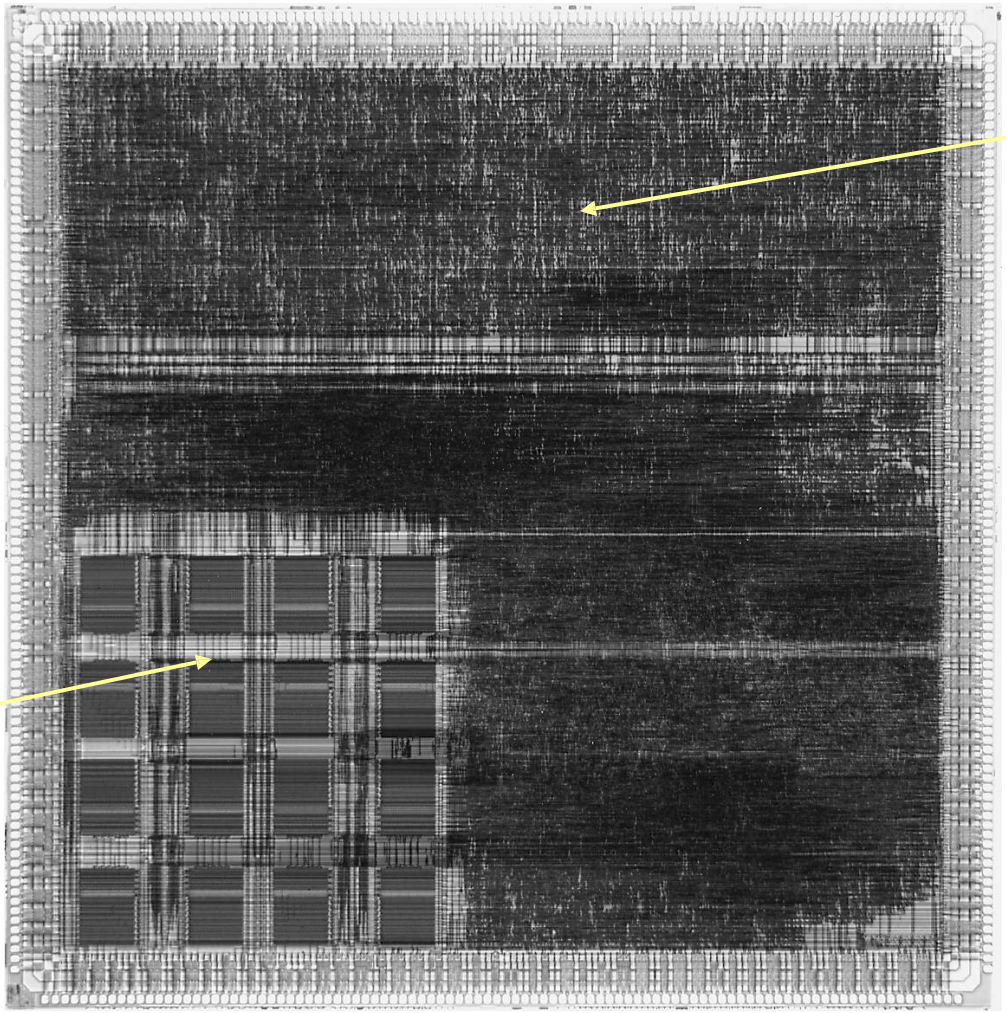



Using oxide-isolation




Using gate-isolation

# Sea-of-gates



Random Logic

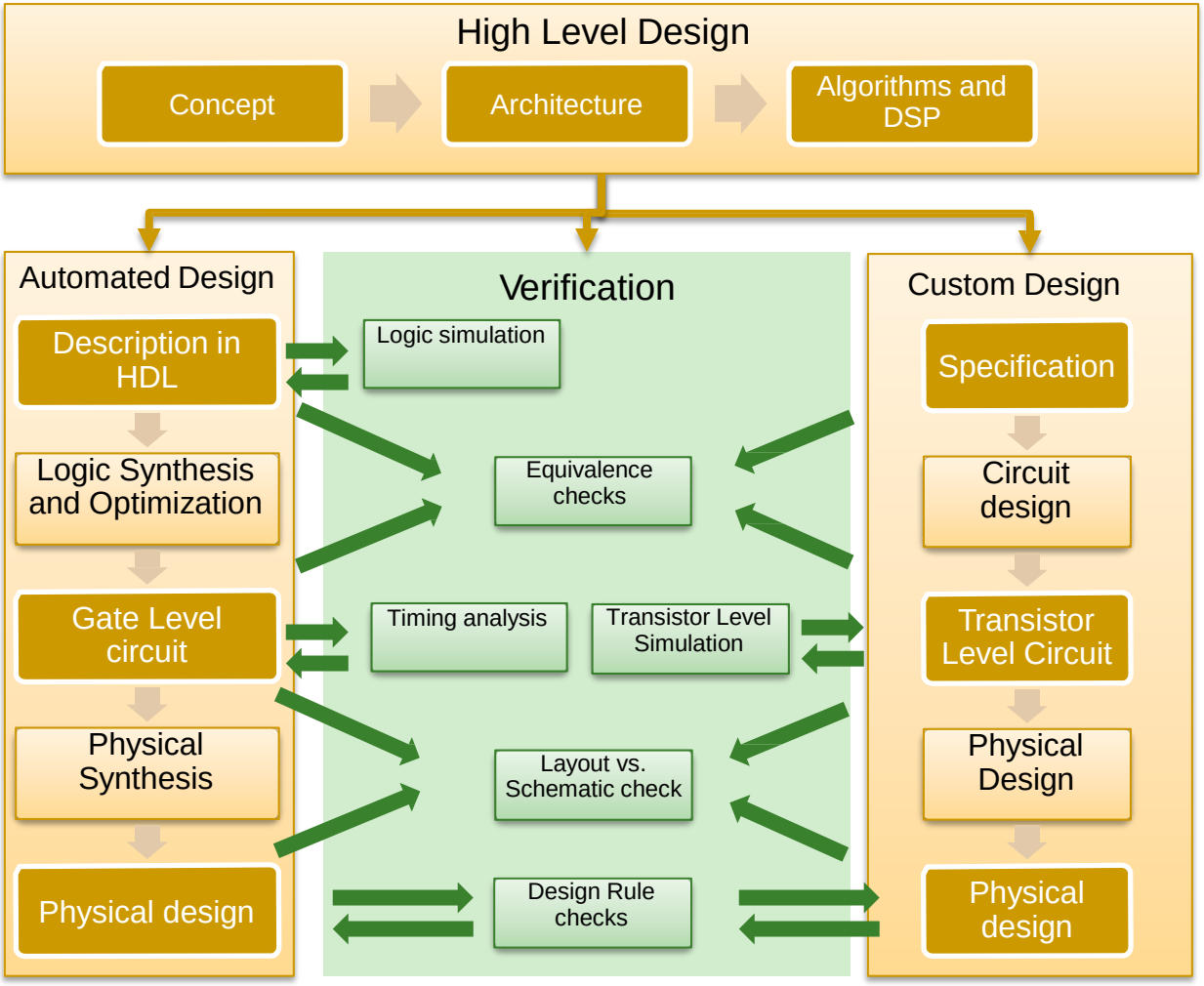
Memory Subsystem

LSI Logic LEA300K (0.6 μm CMOS)

# Implementación de Sistemas Electrónicos

- Un poco de historia, evolución tecnológica
- Fabricación y diseño de C.I CMOS.
- Opciones de diseño
- Flujo de Diseño

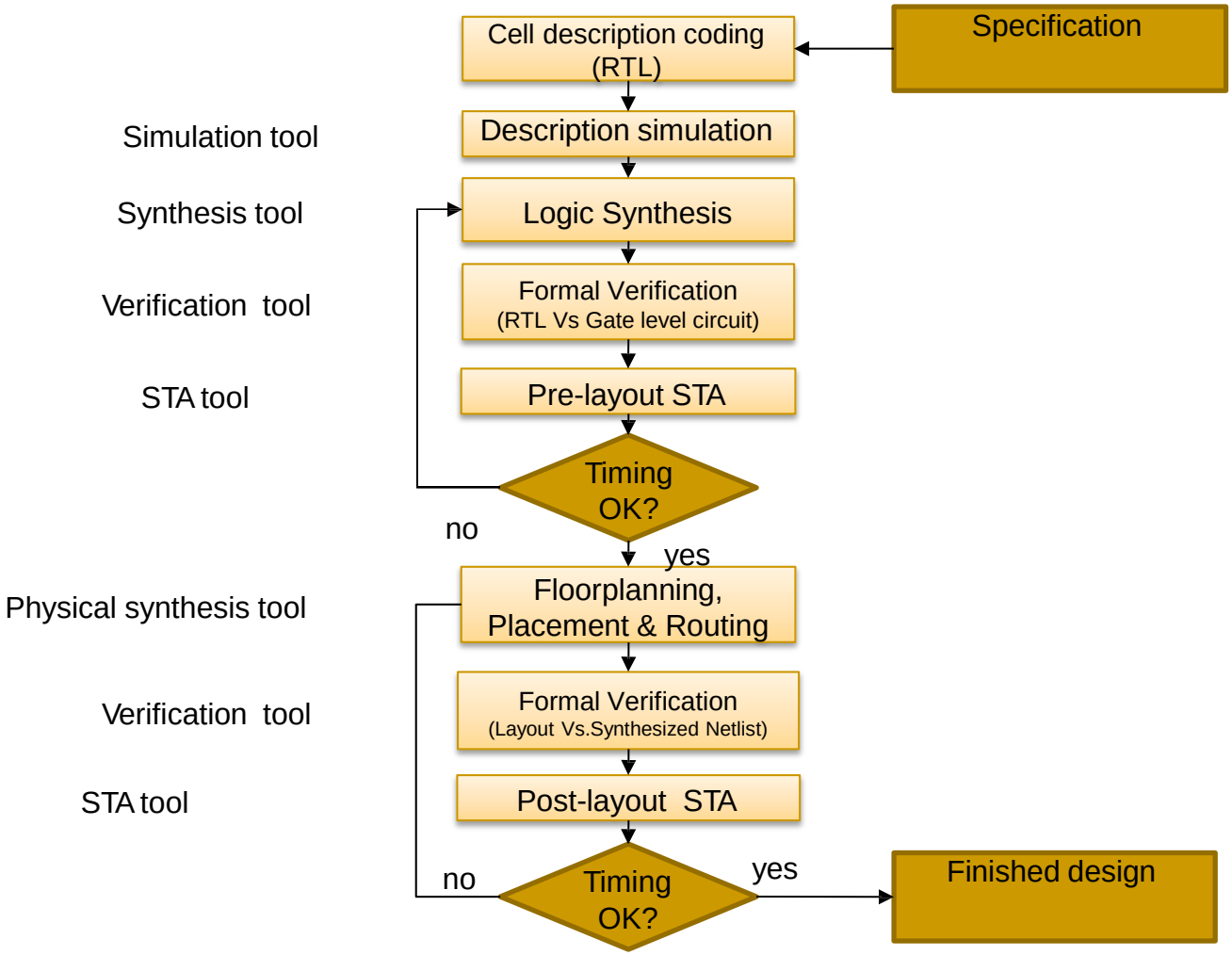
# Concept-to-Silicon Design Flow





EDA Tools
Lecture - 1
Developed By:Vazgen Melikyan

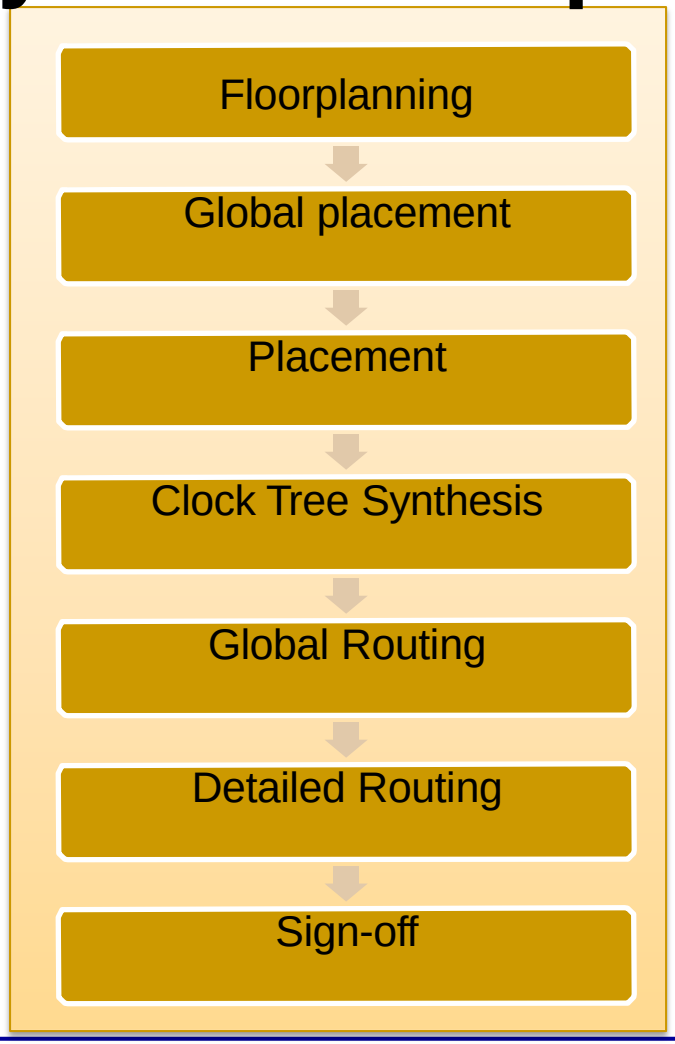
# Digital IC Design Flow



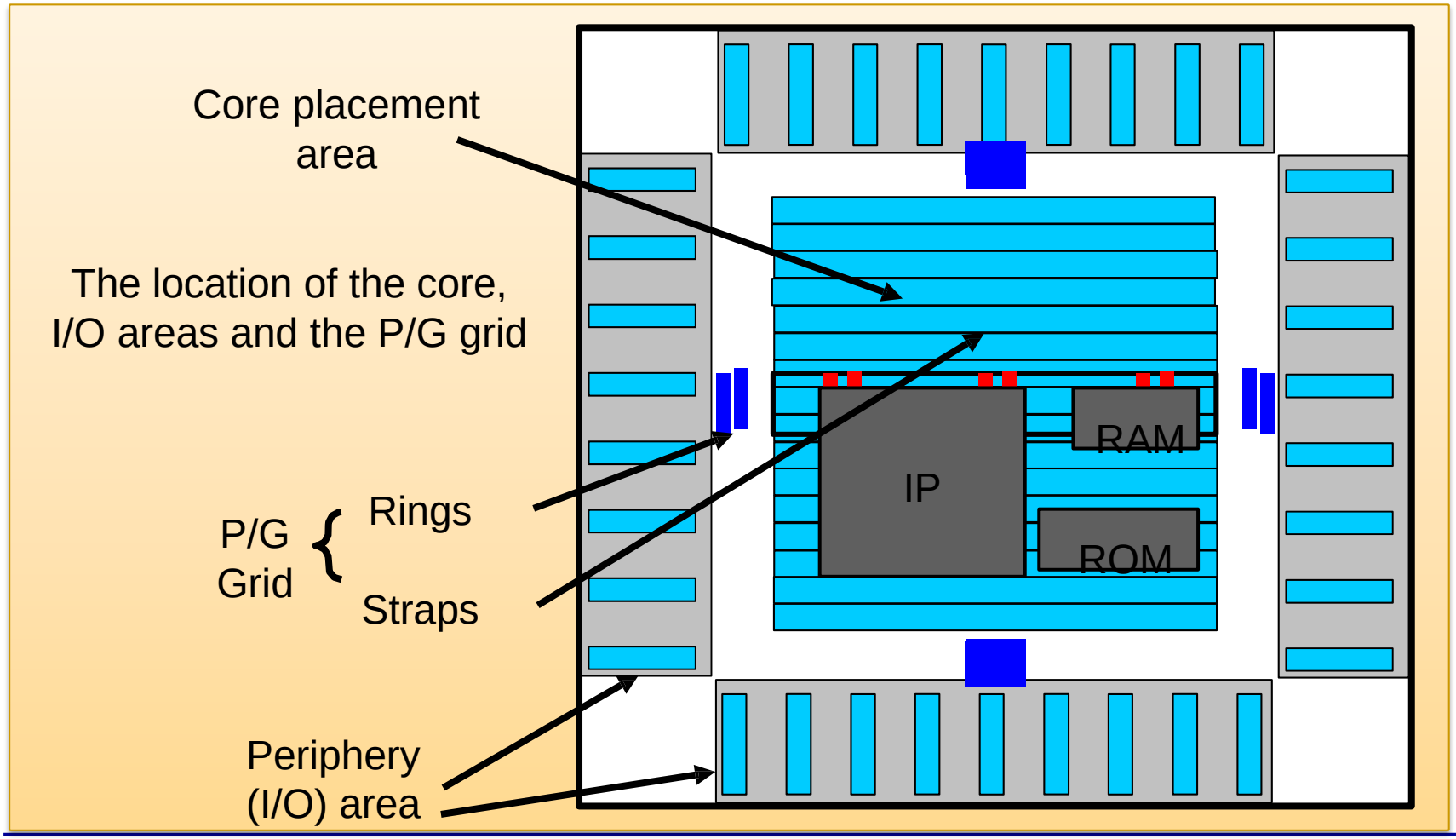


EDA Tools
Lecture - 1
Developed By:Vazgen Melikyan

# Physical Synthesis Steps



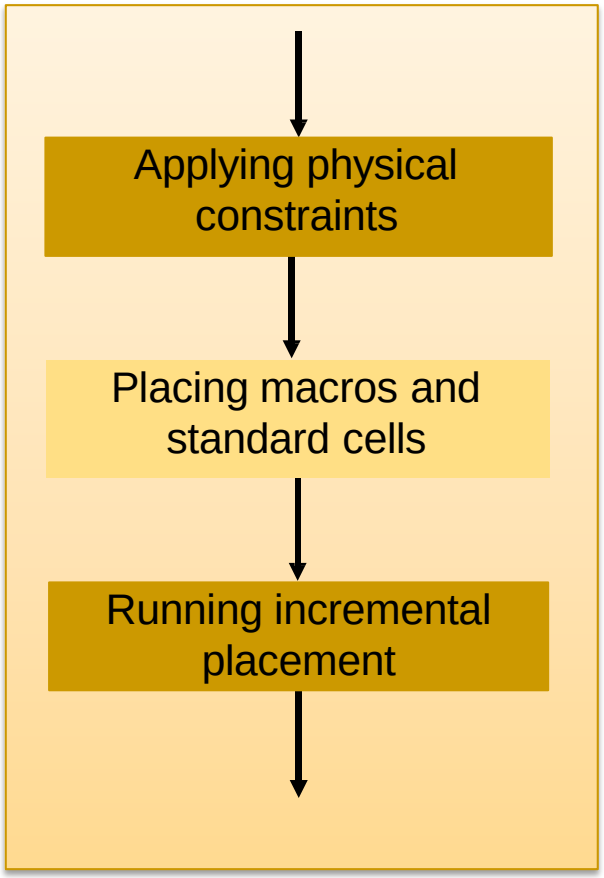
# Floorplanning

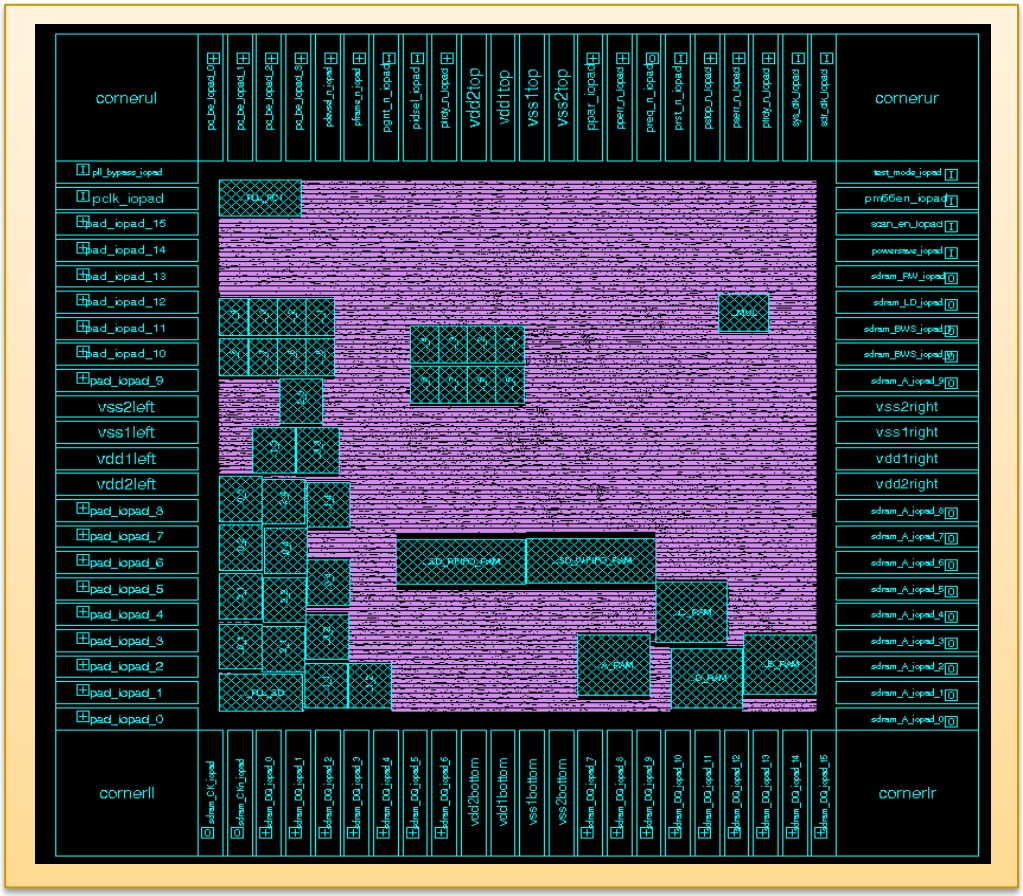




EDA Tools
Lecture - 6
Developed By:Vazgen Melikyan

# Placing Macros and Standard Cells

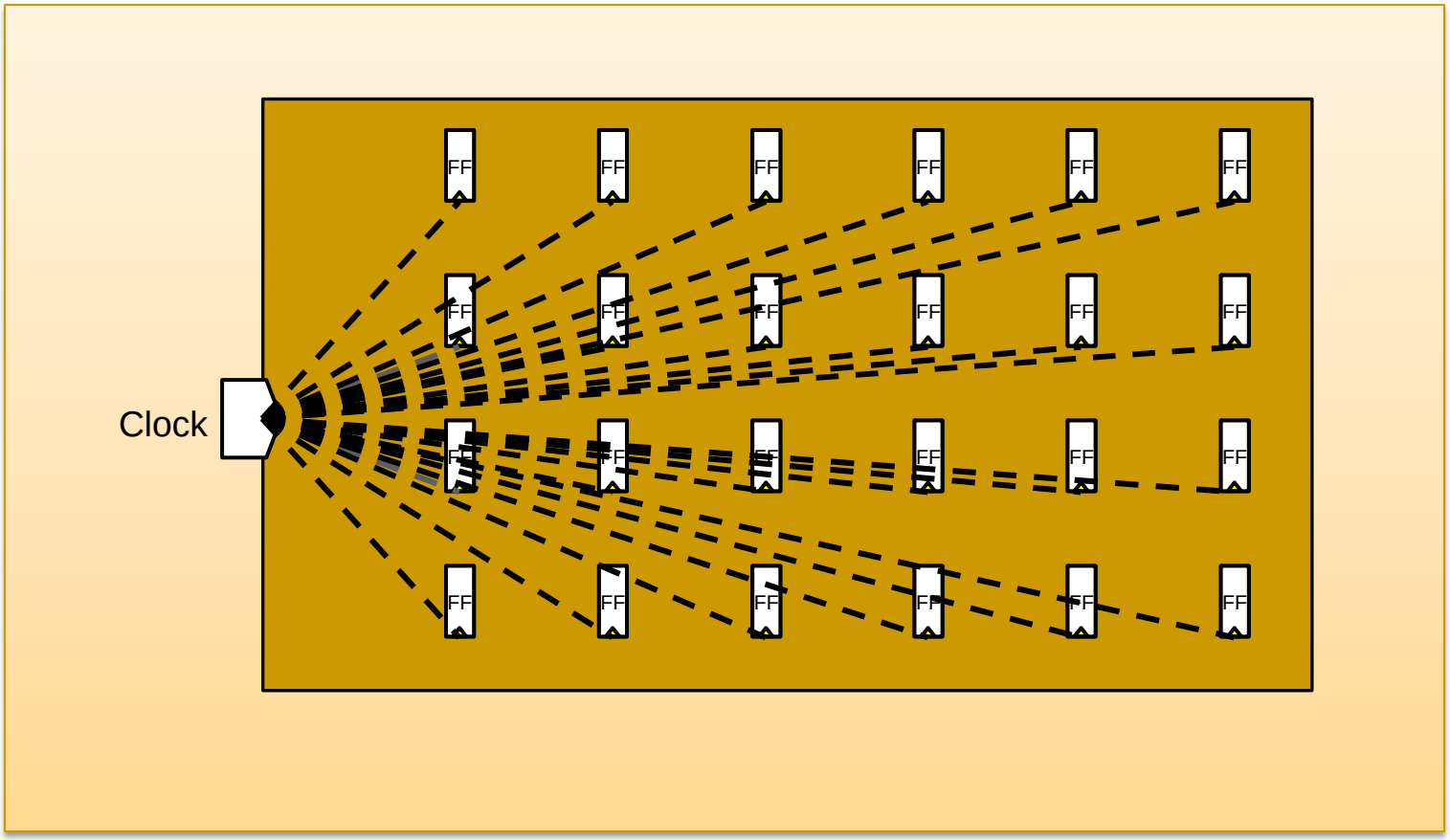


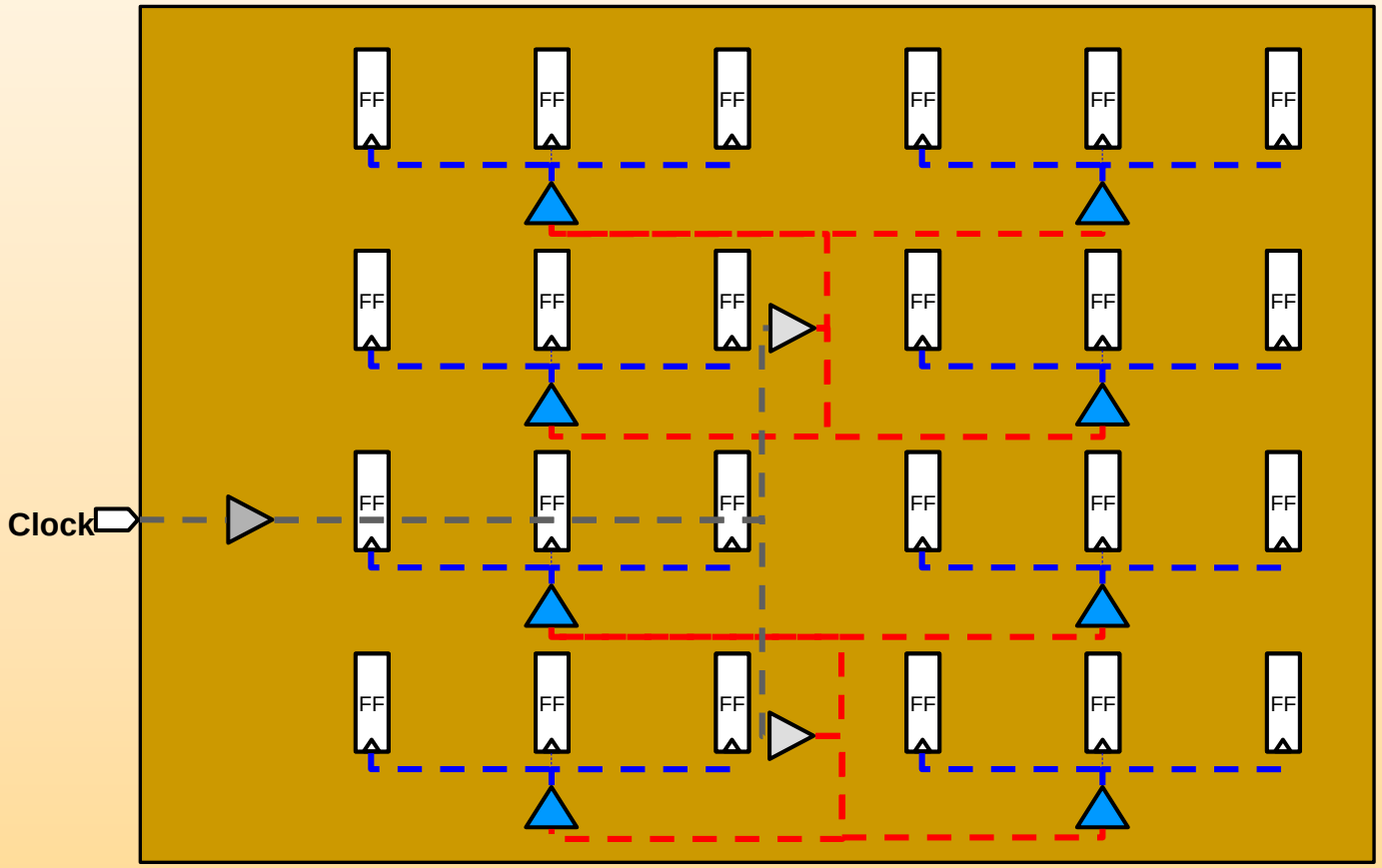


EDA Tools
Lecture - 6
Developed By:Vazgen Melikyan

# Clock Tree Problem



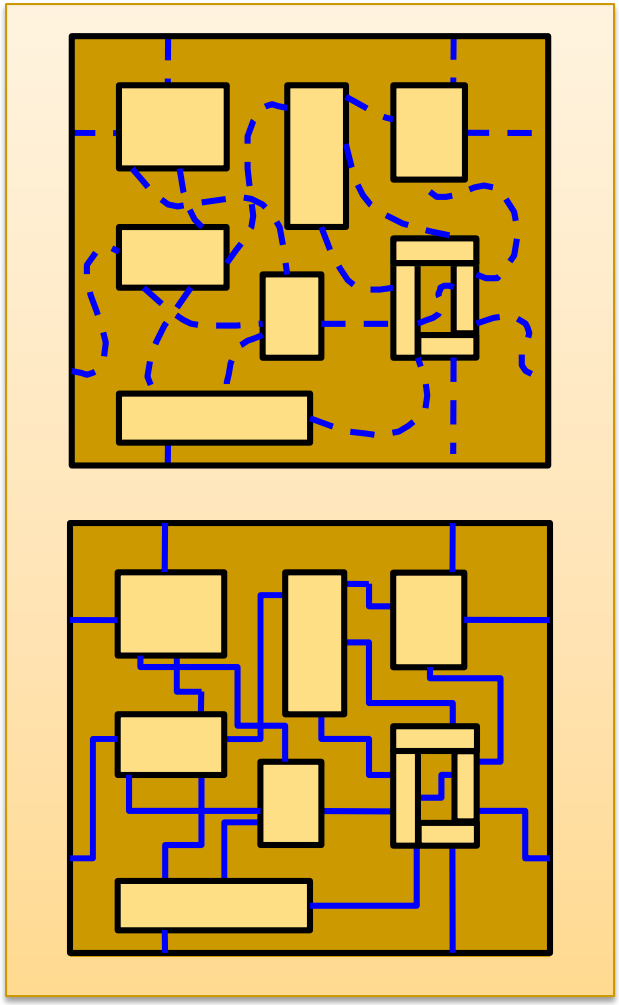
# Clock Tree Synthesis (CTS)



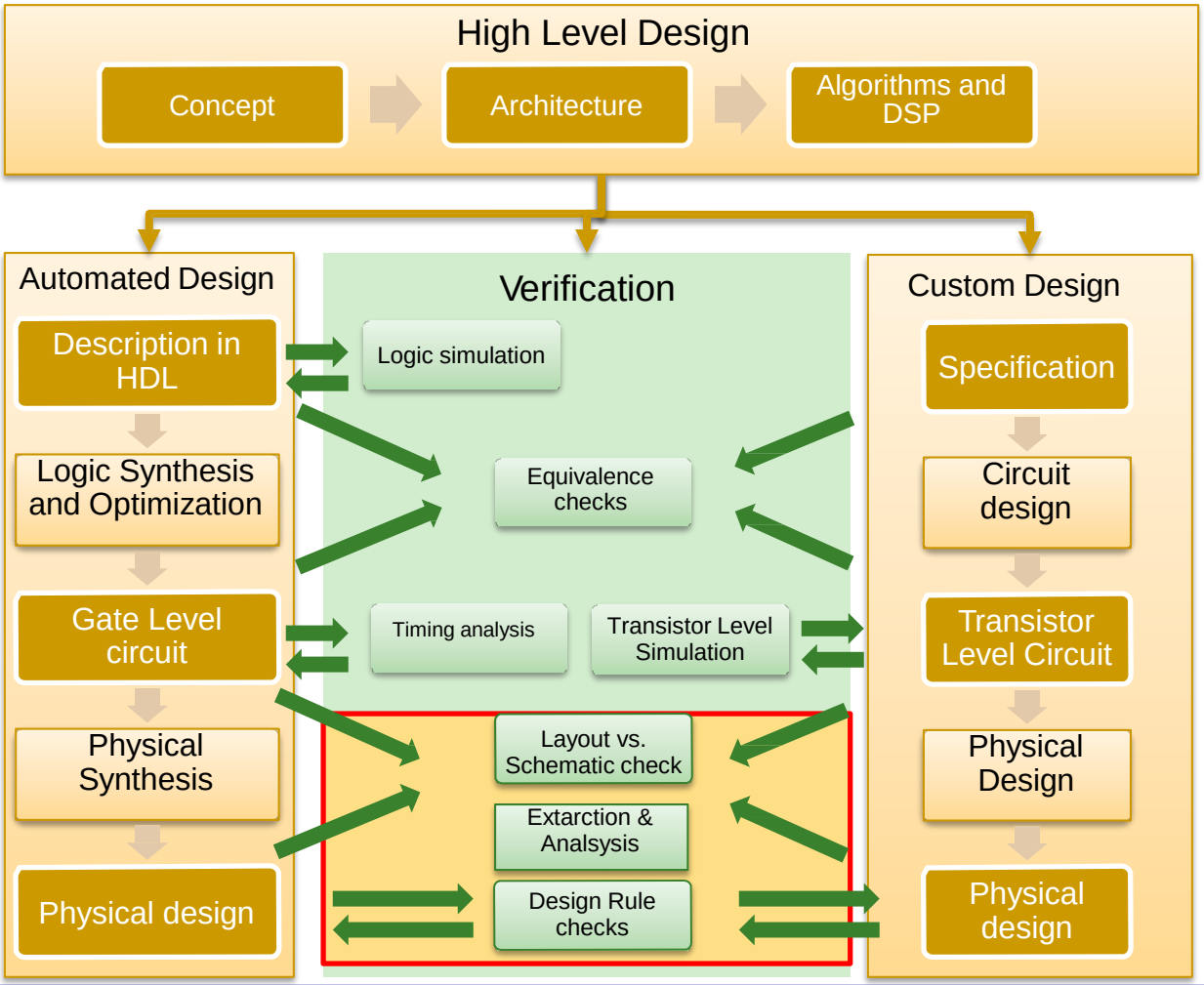

A buffer tree is built to balance the loads and minimize the skew

# Types of Routers

- Global routers
  - function
    - determining routing areas
    - assigning net to routing areas
    - minimizing global routing area, path lengths
  - congestion, approximate path length
- Detail routers
  - goal
    - routing actual wires
    - minimizing routing area, path lengths
  - general-purpose - maze, line probe
  - restricted -channel, switchbox, river routers
- Specialized
  - power, clock routers



# Concept-to-Silicon Design Flow

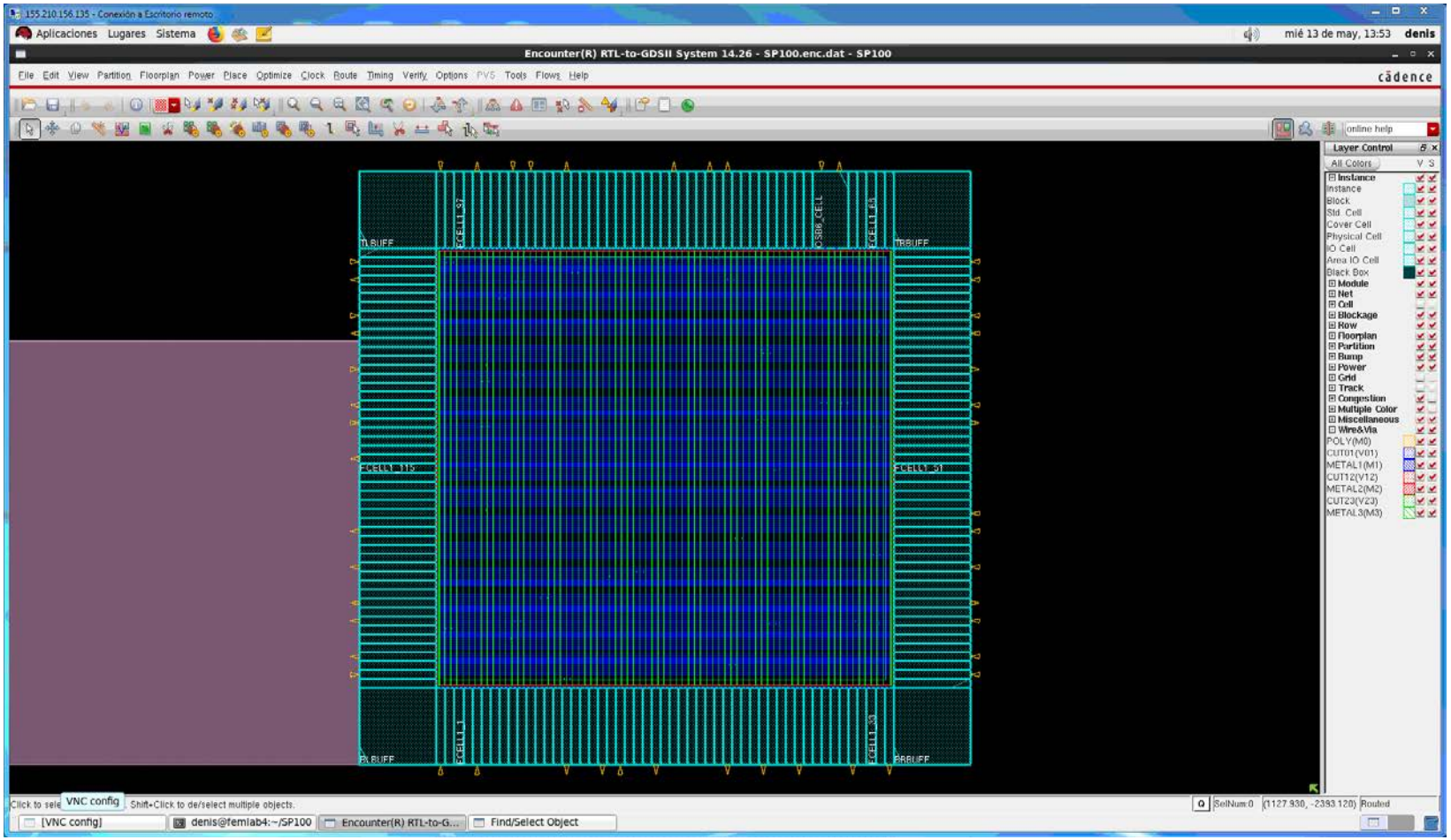




EDA Tools
Lecture - 7
Developed By:Vazgen Melikyan

# DEMO

https://drive.google.com/file/d/1JrvboKfAnk0PNHtWe695EF_k2hFIvfqf/view?usp=sharing

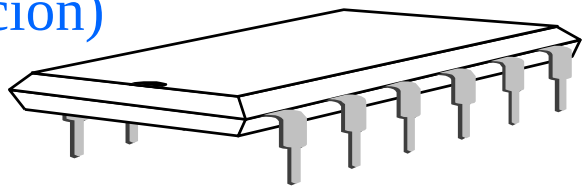


# VERIFICACION

- Test Funcional
  - Estudio estímulo-respuesta
  - Simulador lógico

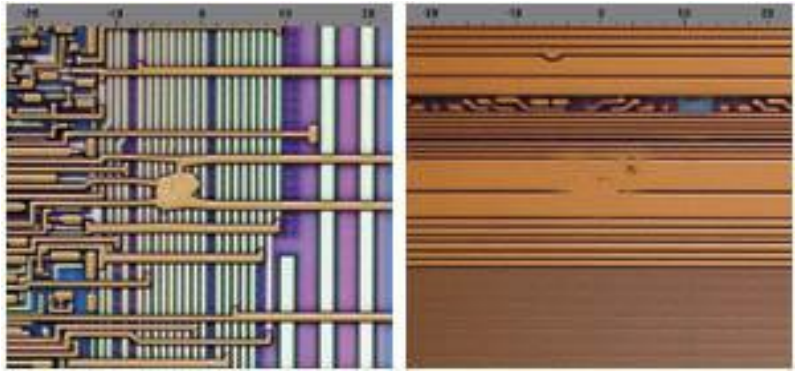
- Análisis temporal
  - Cálculo directo de tiempos entre la salida de un biestable y la entrada del
    siguiente (suponiendo el diseño síncrono)
    - Tiempos de propagación
    - Tiempos hold y set-up

- Test de Circuitos Integrados (Fabricación)

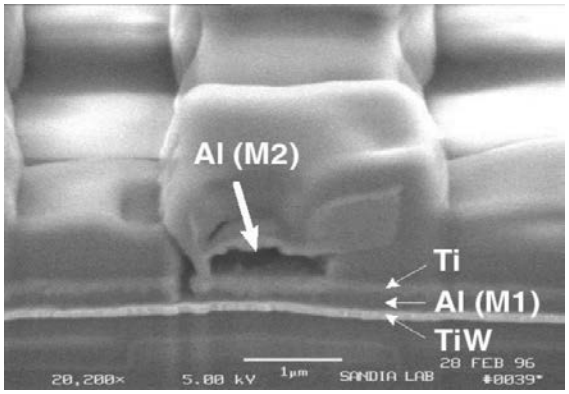


  - ¿Está este circuito bien fabricado?

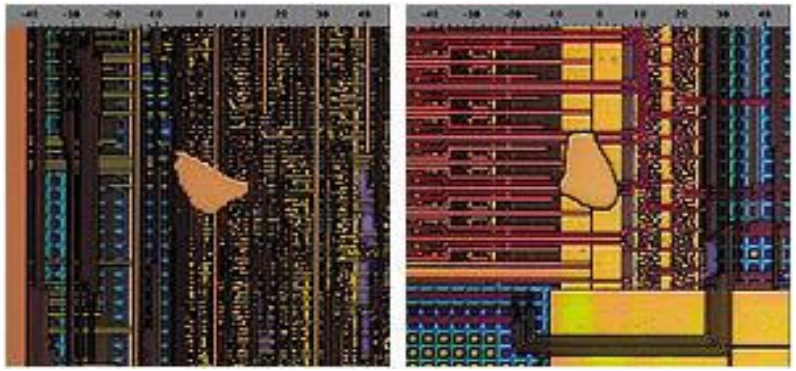
# Catastrophic defects



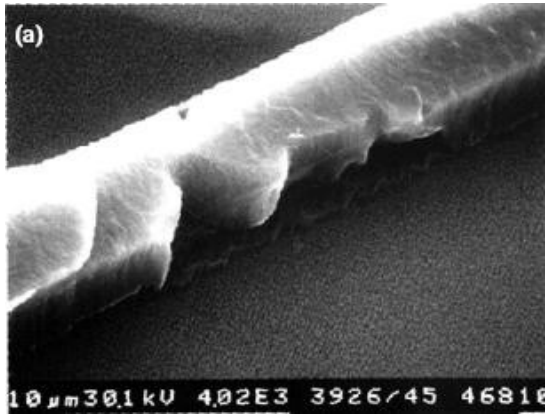
bridge formation (DRAM) - optical




defective via (void in Al layer) - SEM



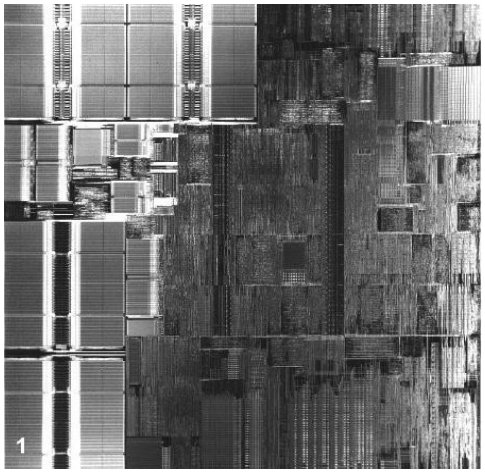
residual particle masked the metal-etch process - optical



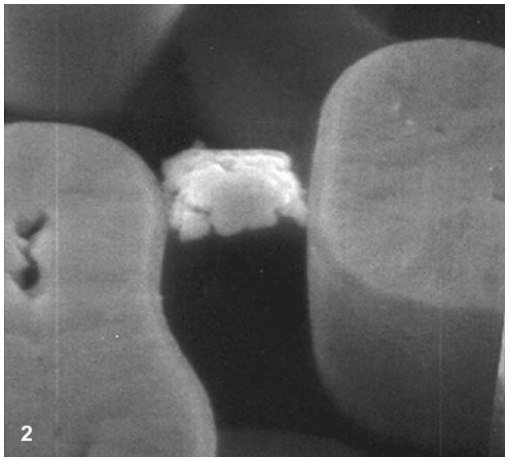

electromigration notch

Sources: T. Reuter, *et al* , Using laser-based patterned-wafer inspection for memory and logic applications; J. M. Soden, *et al*, IC Failure Analysis: Magic, Mystery, and Science; C. F. Hawkins, *et al*, Test and Reliability: Partners in IC Manufacturing, Part 1

# Ejemplo




>5M transistor microprocessor, its surface is 196mm2, it has 5 levels of wiring




0.2μ m x 0.4μ m nickel particle causing a short between two nodes

Sources: D. P. Vallett, IC Failure Analysis: The Importance of Test and Diagnostics